Portable Cost-Effective 3D Digital AESA Radar – Technology Development and Its Impact on EW

Speaker:
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Chairmen & C.E.O, Tron Future Tech Inc.
Our Mission:
• We help our customers collect, analyze and utilize valuable data through fundamental sensor and communication inventions.

Area of Focus:
• Ultrathin all-digital/hybrid phased array based radar/communication turnkey systems.
• Value-added data processing infrastructure.

Our Taiwanese customers in 2019:
• National Space Program Office.
• R.O.C. Military.
• Changhua offshore wind farms. (via. Hong-Yi Ecological Co., Ltd.)

About Us:
>30% employee with Ph.D. degrees from Caltech/USC/MIT/UCLA/NTU/NCTU/NTHU etc.

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Agenda

• Summary from Our EW Europe 2018/EW Asia 2019 Talks

• AESA Cost Reduction and Trade-offs

• Cost-Effective AESA and Initial Experimental Results

• Implications and Conclusions
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Wireless Scanning Technology Development

### AESA
Active Electronically Scanned Array

### PESA
Passive Electronically Scanned Array

### Mechanically Scanned Antenna
- TWT Based
- Solid-State Based

<table>
<thead>
<tr>
<th>Mechanically Scanned Antenna</th>
<th>Electronically Scanned Array</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single RF Transceiver</td>
<td>Multiple RF Transceiver</td>
</tr>
</tbody>
</table>

#### AESA vs. PESA
- **Analog AESA**: Low Analog Complexity (RF Transceiver)
- **Hybrid AESA**: Moderate Analog Complexity + High Digital Complexity (Digital Signal Process)
- **All-Digital AESA**: Low Analog Complexity + High Digital Complexity (Digital Signal Process)

Ref: EW Asia 2019: "Ultrathin All-Digital Software-defined Active Phased Array Technology"
Ultrathin Form Factor

• AESA size can only be shrank by thickness.

• What is drives for ultrathin form factor?
  1. Light weight, small volume → portable.
  2. Lower BOM/material usage → cost in long run.

• What breakthroughs have been made in technology?
  1. Arithmetic and Logic Circuit → 80x size & performance improvement in last 12 years.
  2. Analog-to-Digital Converter → 5x size & power improvement in 10 years.
  3. RF Power Amplifier → GaN PA generates 10x more power with >50% efficiency.
  4. Transceiver Modules → discrete to integrated TR module, >100 times size reduction.
  5. Packaging and Assembling → 3D-IC-stacking ball grid array (BGA) with flip-chip process.

Ref: Our EW Europe 2018 Talk:” Flexibility and Thinness – How Semiconductor Technologies Shape Future Radar and Electronic Warfare?”
Scalable Subarray (4x4)

Subarray Architecture

Top View

Side View

Expect ~20mm thickness in 2020.
The RF SoC can work with several GaAs and GaN frontends (LNA/PA).

Production test approaches are proposed and reported in PIERS 2018.

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**Operational Frequency**
- Band: 9-10 GHz
- Channel BW: 40 MHz

**A Typical GaAs Frontend**
- PA Power: 27 dBm
- LNA Gain: 16 dB
- LNA NF: 2.5 dB
- Switch Time: 1 ns

**CMOS RF SoC**

<table>
<thead>
<tr>
<th>Transmitter</th>
<th>Receiver</th>
</tr>
</thead>
<tbody>
<tr>
<td>Digital Input</td>
<td>RF Input</td>
</tr>
<tr>
<td>RF Output</td>
<td>Digital Output</td>
</tr>
</tbody>
</table>

**Synchronized CLK Distribution**

**Package Size**
- 15.3 mm x 15.3 mm x 3 mm
- 2.6 mm (assembled thickness)
4x8 Array Pattern Measurement
- Measured peak EIRP ~ 48 dBm with 32 CMOS only TXs.
- Expected: 66dBm with 32 CMOS TXs + 32 GaN PAs.

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AESA Radar Cost Source: (1) Phased Array

Phased array is a highly repetitive structure. The performance is proportional to the array size.

The cost of phased array is proportional to the total no. of array elements and PA power.

AESA Radar Cost Source: (2) Thermal Cooling

- Air-cooling has a heat density limit \( \sim 10\text{kW/m}^2 \).
- Liquid-cooling removes 20~50 times more heat with 4~10 times the cost.

Today’s AESAs use Commercial Off-The-Shelf (COTS) devices such as FPGA, GPU, CPUs.
Digital AESA will increase computing power requirements, but we get lots of additional benefits in return. We expect the processor cost to increase in the future.
NRE cost for 130nm process is ~$200K, while 16nm > $3M.
### AESA Radar Cost Structure Example

#### Tile Arrays at S-band with 10W-PA

<table>
<thead>
<tr>
<th>Phased Array Radar Cost Sources</th>
<th>$/m²</th>
</tr>
</thead>
<tbody>
<tr>
<td>T/R Module</td>
<td>$80,000</td>
</tr>
<tr>
<td>T/R Module Packages</td>
<td>$5,000</td>
</tr>
<tr>
<td>RF Board</td>
<td>$25,000</td>
</tr>
<tr>
<td>Cable &amp; Connectors</td>
<td>$1,000</td>
</tr>
<tr>
<td>Structure</td>
<td>$15,000</td>
</tr>
<tr>
<td>Assembly &amp; Test</td>
<td>$15,000</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>$200,000</strong></td>
</tr>
</tbody>
</table>

- **Thermal Cooling**: $40,000
- **Digital Processor**: $20,000

**Total**: $200,000

- Only hardware production cost is considered.
- Software, field test expenses and other NRE are not listed.
- To dramatically reduce AESA cost, we need to dramatically reduce no. of elements.

Cost Reduction and Sidelobes Issues

- N=512 $\Rightarrow$ N=64
  - Peak Power Reduced.
  - Mainlobe beamwidth Increased.
  - Sidelobe Increased.
- Why sidelobes matter?
  - False targets.
- Though we can still distinguish range and velocity (MTI) bins.
Digital Beamforming v.s. Analog Beamforming

- Typical analog elementary errors:
  - $\pm 1\text{dB}$ amplitude variation, $\pm 3^\circ$ phase error.

- All digital array achieve similar level of sidelobe rejection using 2~10 times less elements than analog counterparts.
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3D AESA Cost Reduction

- Fully Populated Planar AESA.
- Orthogonal Linear Digital AESA.

<table>
<thead>
<tr>
<th></th>
<th>No. of Elements</th>
<th>Peak Power</th>
<th>Antenna Gain</th>
<th>Max. Dwell Time</th>
<th>SNR</th>
<th>Cost per Area</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$W \times H$</td>
<td>$P_0 \times W \times H$</td>
<td>$\propto W \times H$</td>
<td>$T_0$</td>
<td>$SNR_0$</td>
<td>$C_0$</td>
</tr>
<tr>
<td></td>
<td>$H$ (TX), $W$ (RX)</td>
<td>$\sim P_0 \times (H)$</td>
<td>$\propto W$ (RX), $\propto H$ (TX)</td>
<td>$T_0 \times H$</td>
<td>$SNR_0 \cdot H/H^3$</td>
<td>$C_0 \cdot H/H^3$</td>
</tr>
</tbody>
</table>

- $1024 \rightarrow 32$ (3% cost)
- 3% original power
- 3% gain for RX & TX
- 32 times with RX multibeam
- $1/1024 \rightarrow (18\%$ detection range)
- Similar cost per coverage area.

Comparable side-lobe suppression, mainlobe.
Basic Operational Concepts

- Transmitter fan-shaped pattern.
- Receiver multi-beam pattern.
- Equivalent transmit-to-receive patterns.
- TX Vertical Scanning.
- RX Horizontal Multibeam Scanning.
- Equivalent Radar Beam Pattern

This is not the only operations, but a working example to show how it can work.
## The Cost-Effective AESA Prototype

### Specifications

<table>
<thead>
<tr>
<th>Specification</th>
<th>Details</th>
</tr>
</thead>
</table>
| Number of Elements                     | 1×16 TX (CMOS array with GaN PAs\(^*\))  
1×16 RX (CMOS array with GaN LNAs\(^*\)) |
| Architecture                           | Two hierarchy AESA                                                                          |
| Frequency                              | 8-9.5 GHz                                                                                   |
| Phase-shifting                         | All-digital                                                                                 |
| Applications                           | Radar/Communication/EW                                                                      |
| Size (W/ Structure)                    | 63 cm x 63 cm x 13 cm                                                                      |
| Antenna Size (W/O Separator)           | 1×16 TX\(^**\): 31.7 cm x 7.03 cm  
1×16 RX\(^**\): 31.7 cm x 7.75 cm |
| Weight (W/O Structure)                 | 2.545 kg                                                                                    |
| Angular Scanning Range                 | ±60° (RX) / ±45° (TX)                                                                       |
| Peak EIRP                              | 63 dBm                                                                                      |
| Only two external interface            | 1. AC Power: 90-230 VAC (Optional 20-60V VDC) 700W peak.  
2. Ethernet.                           |

\(^*\) GaN PA: Qorvo TGA 2598; GaN LNA: Qorvo TGA 2512  
\(^**\) 1×16 frontend has two dummy antenna beside the main 16 antennae.

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This slide contain proprietary information which is currently U.S. patent pending.
1TX 16RX LFM Multibeam Radar Experiments

- Distance: A=924m, B=808.5m, C=721.5m, D=831m, E=1101m, F=382.5m, G=530m

- This experiment used 1 TX and the 16-element RX array is located at 7F (around 35m from the ground).
- An absorber is used in front of the RX to limit the elevation angles so that close-in reflections from the ground are not received.
- The transmit pulse is 32 uSec LFM, and received signal is averaged by 64 PRIs, and then passes through the matched filter of the LFM signal.
1TX 16RX LFM Multibeam Radar Experiments

- From the top view, it is found that the light spots in the result plots of the experiment are perfectly matched to the buildings shown on a map of the local area (map data from Google map).

- The farthest range of this experiment is \((768\text{pt}-32\text{pt})\times1.5 = 1104\text{m}\).
16TX 16RX 3D Surveillance Experiments

Pitch Angle: 30°
3D Drone Tracking Example

- Drone: DJI Phantom 4 (~0.01m² RCS)
Most Likely S/X-band AESA Production Spec.

S-band (2.9-3.1GHz)

<table>
<thead>
<tr>
<th>No. of Elements</th>
<th>32 TX, 32-48 RX (TBD)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Peak EIRP</td>
<td>25kW</td>
</tr>
<tr>
<td>Weight</td>
<td>&lt;20kG</td>
</tr>
<tr>
<td>Est. Power Consumption</td>
<td>~200W</td>
</tr>
<tr>
<td>Beamwidth</td>
<td>3.5°(H), 7°(V)</td>
</tr>
<tr>
<td>Simulated Range</td>
<td>&gt;20km@2m², 2Hz Tracking</td>
</tr>
<tr>
<td>First Shipping for Field Test</td>
<td>Sept. 30, 2019</td>
</tr>
</tbody>
</table>

X-band (8.0-9.5GHz)

<table>
<thead>
<tr>
<th>No. of Elements</th>
<th>64 TX, 64-96 RX (TBD)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Peak EIRP</td>
<td>20kW</td>
</tr>
<tr>
<td>Weight</td>
<td>&lt;15kG</td>
</tr>
<tr>
<td>Est. Power Consumption</td>
<td>~150W (TBD)</td>
</tr>
<tr>
<td>Beamwidth</td>
<td>2°(H), 3.5°(V)</td>
</tr>
<tr>
<td>Simulated Range</td>
<td>&gt;10km@2m², 2Hz Tracking</td>
</tr>
<tr>
<td>First Shipping for Field Test</td>
<td>TBD</td>
</tr>
</tbody>
</table>

This slide contain proprietary information which is currently U.S. patent pending.
Cost-effective AESAs begin to be pervasive to complement existing high-performance AESAs.

Chip-scale atomic clocks enable massive software-defined AESA platform.

Software is key to fully utilize the massive number of AESA.
• Global temporal-spatial database in the cloud keeps track of area being serviced and tracking data from each AESA.
• Each AESA checks out a region from the cloud, and run autonomously. Keep updating operating status to the cloud. The cloud arbiter/resolves any conflicts from each AESA.
• Cooperation between a large number of mobile AESA and conventional units while making the whole system resilient and robust with redundant units will be an important problem that needs to be extensively studied.

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Conclusion

• AESA hardware cost is roughly proportional to array elements.

• Reducing array elements will reduce peak power (range), increase mainlobe beamwidth (number of identified targets), and reduce sidelobe rejection. Sidelobe rejection is important for preventing false targets.

• Digital AESA has a much better sidelobe rejection than an analog counterpart.

• Use of orthogonal linear AESAs can create a virtual 2D AESA, but a much smaller number of array elements.

• Reducing array elements, and highly integrated T/R module, we can make mid/short-range AESA light-weight and cost-effective today.

• EW community enters a new era of massive number of AESAs.
Critiques, questions, and suggestions are highly welcome.
Thank you for your attentions.
Email: yw@tronfuturetech.com