Portable Cost-Effective 3D Digital AESA Radar –Technology Development and Its Impact on EW

Speaker:

Dr. Yu-Jiu Wang, (Ph.D., Caltech)

Chairmen & C.E.O, Tron Future Tech Inc.

Tron Future Tech Inc.

About Us:

>30% employee with Ph.D. degrees from Caltech/USC/MIT/UCLA/NTU/NCTU/NTHU etc.

Address:

7F-A, No.1, Sec. 3, Gongdao 5th Rd.,
Hsinchu City 30069, Taiwan, R.O.C.

Our Mission:

- We help our customers collect, analyze and utilize valuable data through fundamental sensor and communication inventions.

Area of Focus:

- Ultrathin all-digital/hybrid phased array based radar/communication turnkey systems.
- Value-added data processing infrastructure.

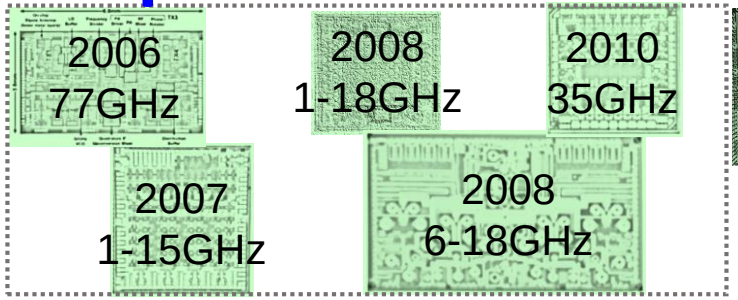
Our Taiwanese customers in 2019:

- National Space Program Office.
- R.O.C. Military.
- Changhua offshore wind farms. (via. Hong-Yi Ecological Co., Ltd.)

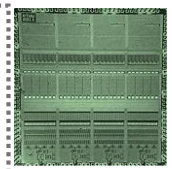
Our Experiences

~ 2008 | ~2010 | 2011 | 2012 | 2013 | 2015 | 2016 | 2017 | 2018 | 2019

Chip Level

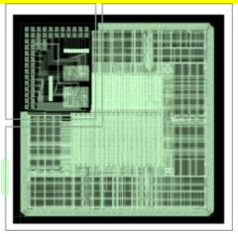


Phased-Array ICs (Participation)

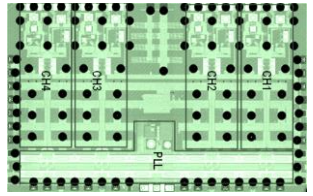


2011
IR Radar

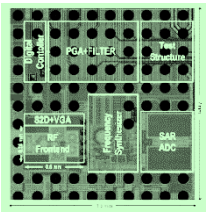
2012
79GHz
Radar



2015 Heterogeneous
Integration Platform



2016 Ka-Band
Phased Array

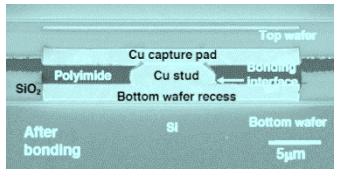


2017 X-band
RF Front-End

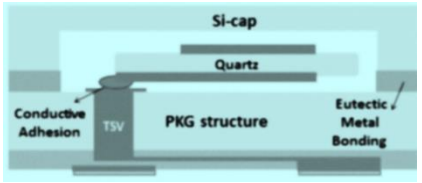
2019 X/S-band
RF Front-End

2019 X/S-band
GaN PA

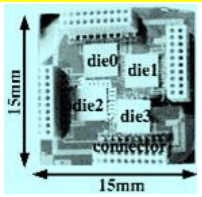
Package Level



2008 3D Device Stacking



2013 Crystal Resonator



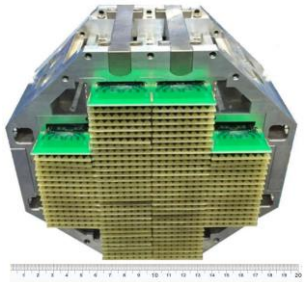
2016 3D Flexible System

2018 Patch
AiP

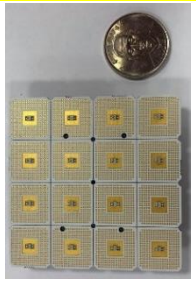
2019 Dual-Pol
Patch AiP

System

Total Solution



2016
35GHz 768-Element
Hybrid AESA



2017
10GHz 16-Element
Digital Subarray

2018
10GHz Digital AESA
Demonstrator

2019 Satellite
Downlink &
SAR Radar

2019 X/S-band
AESA Radar

Data API

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Agenda

- **Summary from Our EW Europe 2018/EW Asia 2019 Talks**
- **AESA Cost Reduction and Trade-offs**
- **Cost-Effective AESA and Initial Experimental Results**
- **Implications and Conclusions**

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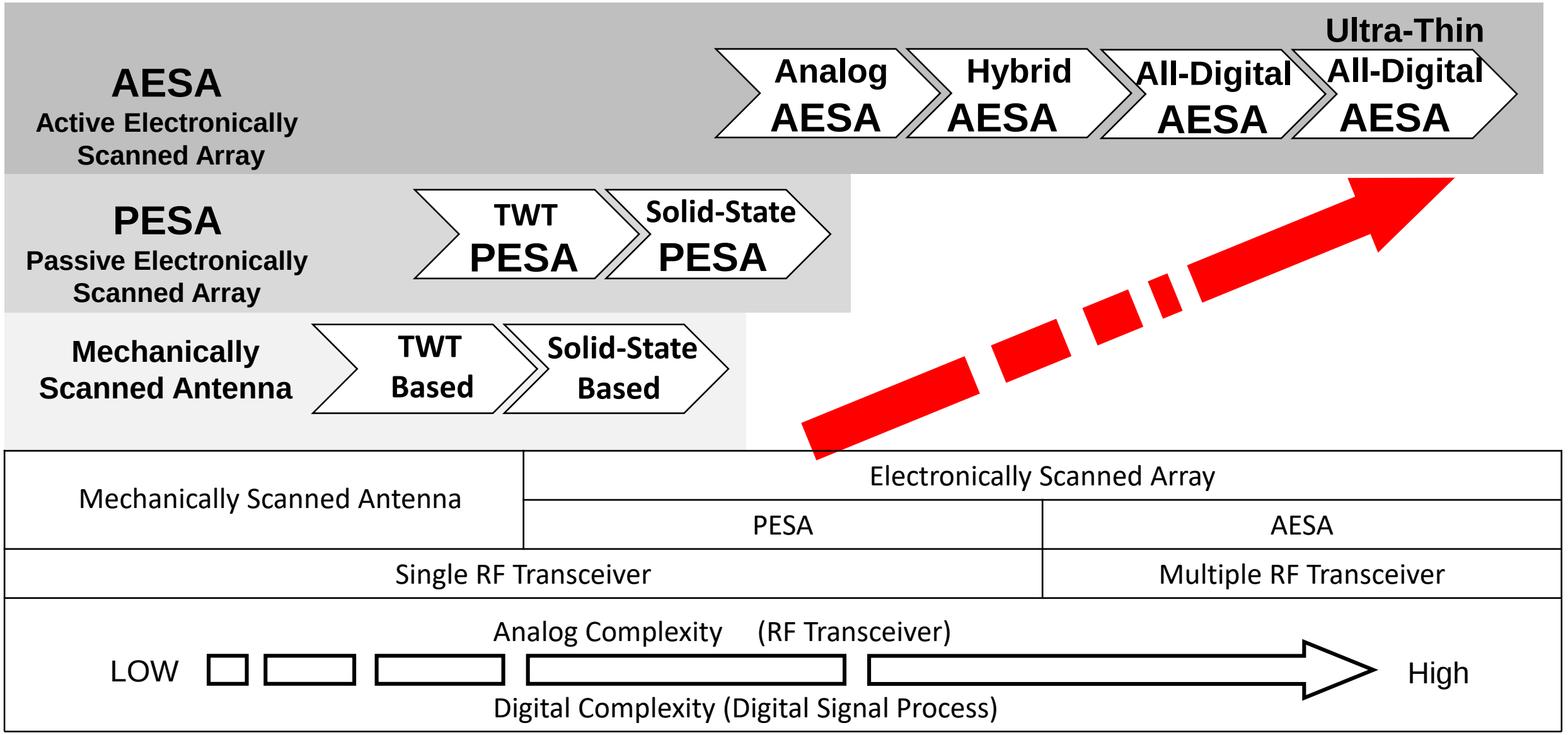
Wireless Scanning Technology Development



Ref: EW Asia 2019:"Ultrathin All-Digital Software-defined Active Phased Array Technology"

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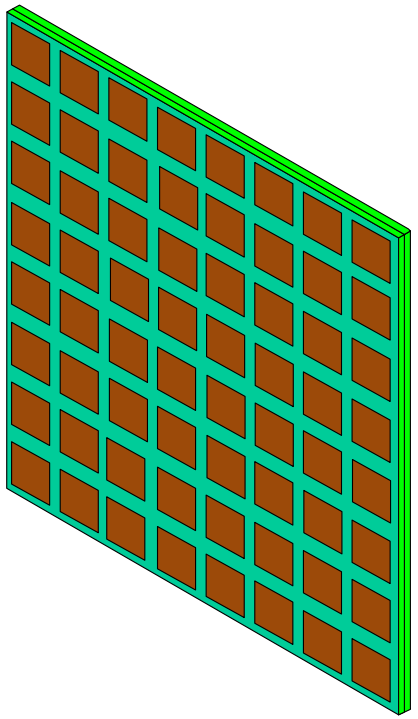
Ultrathin Form Factor



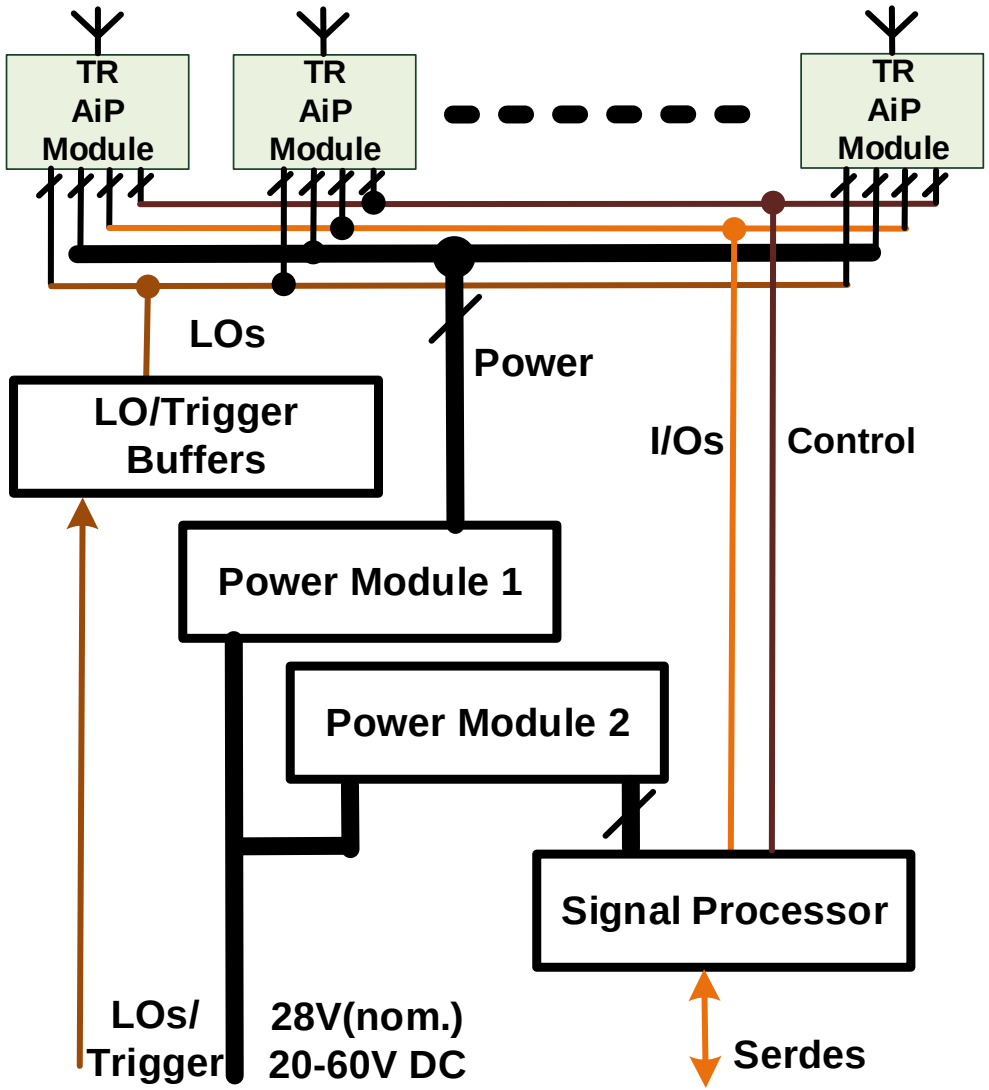
- **AESA size can only be shrank by thickness.**
- **What is drives for ultrathin form factor?**
  1. Light weight, small volume ➔ portable.
  2. Lower BOM/material usage ➔ cost in long run.

- **What breakthroughs have been made in technology?**
  1. **Arithmetic and Logic Circuit** → 80x size & performance improvement in last 12 years.
  2. **Analog-to-Digital Converter** → 5x size & power improvement in 10 years.
  3. **RF Power Amplifier** → GaN PA generates 10x more power with >50% efficiency.
  4. **Transceiver Modules** → discrete to integrated TR module, >100 times size reduction.
  5. **Packaging and Assembling** → 3D-IC-stacking ball grid array (BGA) with flip-chip process.

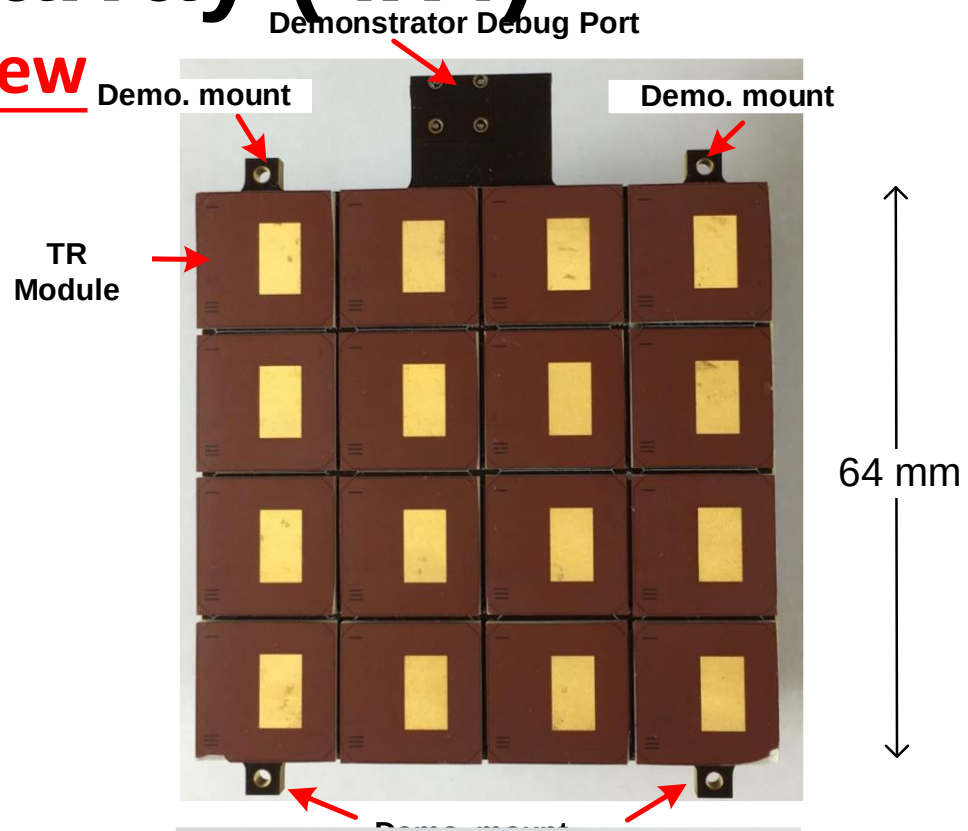
Ref: Our EW Europe 2018 Talk:" Flexibility and Thinness – How Semiconductor Technologies Shape Future Radar and Electronic Warfare?"

Scalable Subarray (4x4)

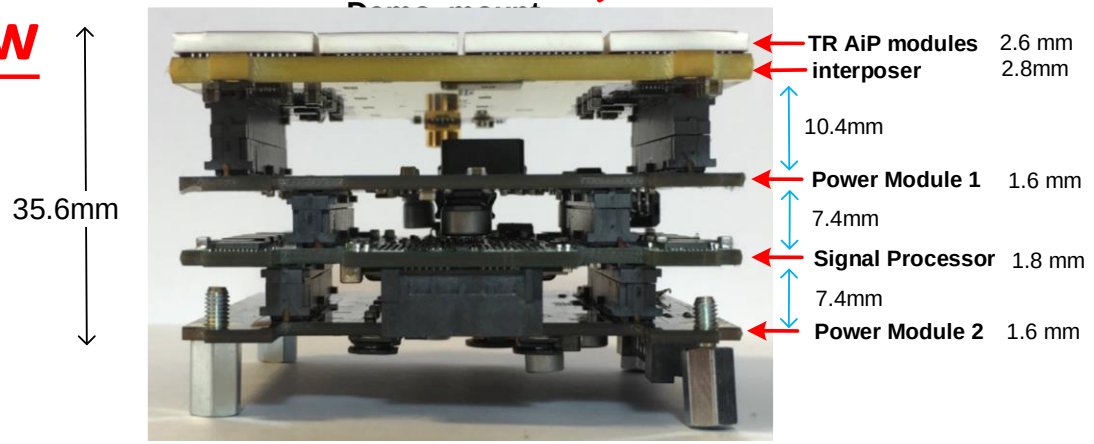
Subarray Architecture



Top View

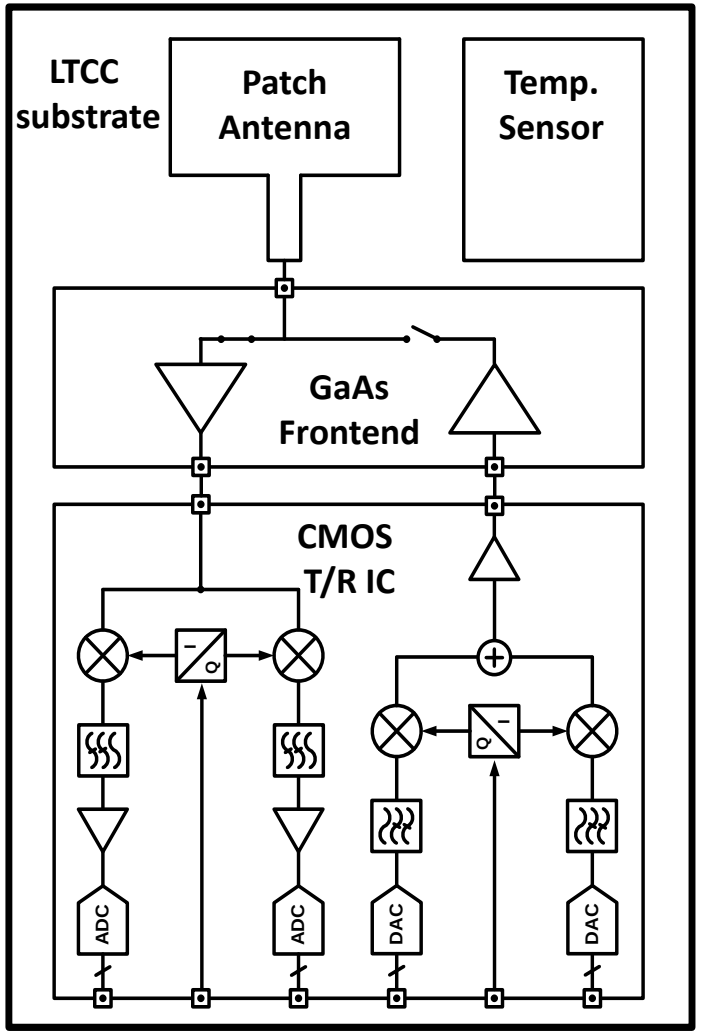


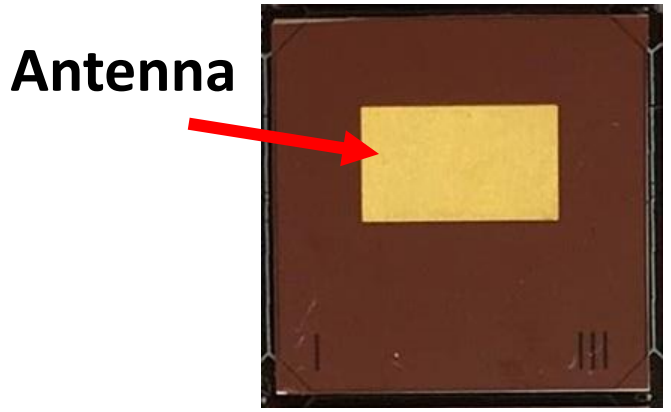
Side View



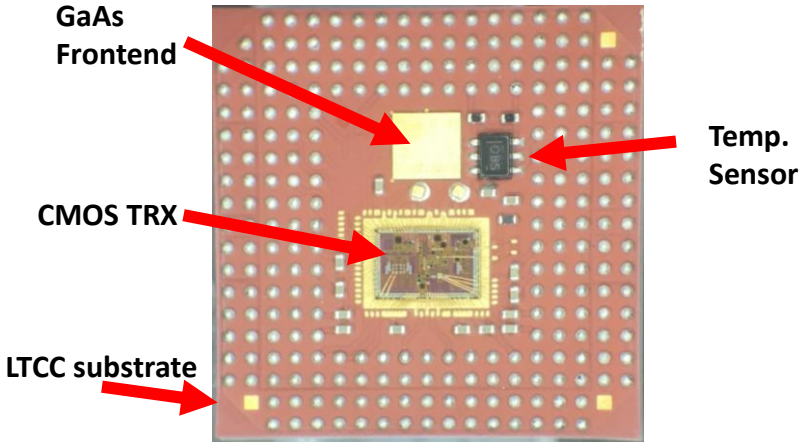
Expect ~20mm thickness in 2020.

The LTCC Multichip TR Modules and AiP





Top View



Bottom View

Operational Frequency
Band: 9-10 GHz
Channel BW: 40 MHz

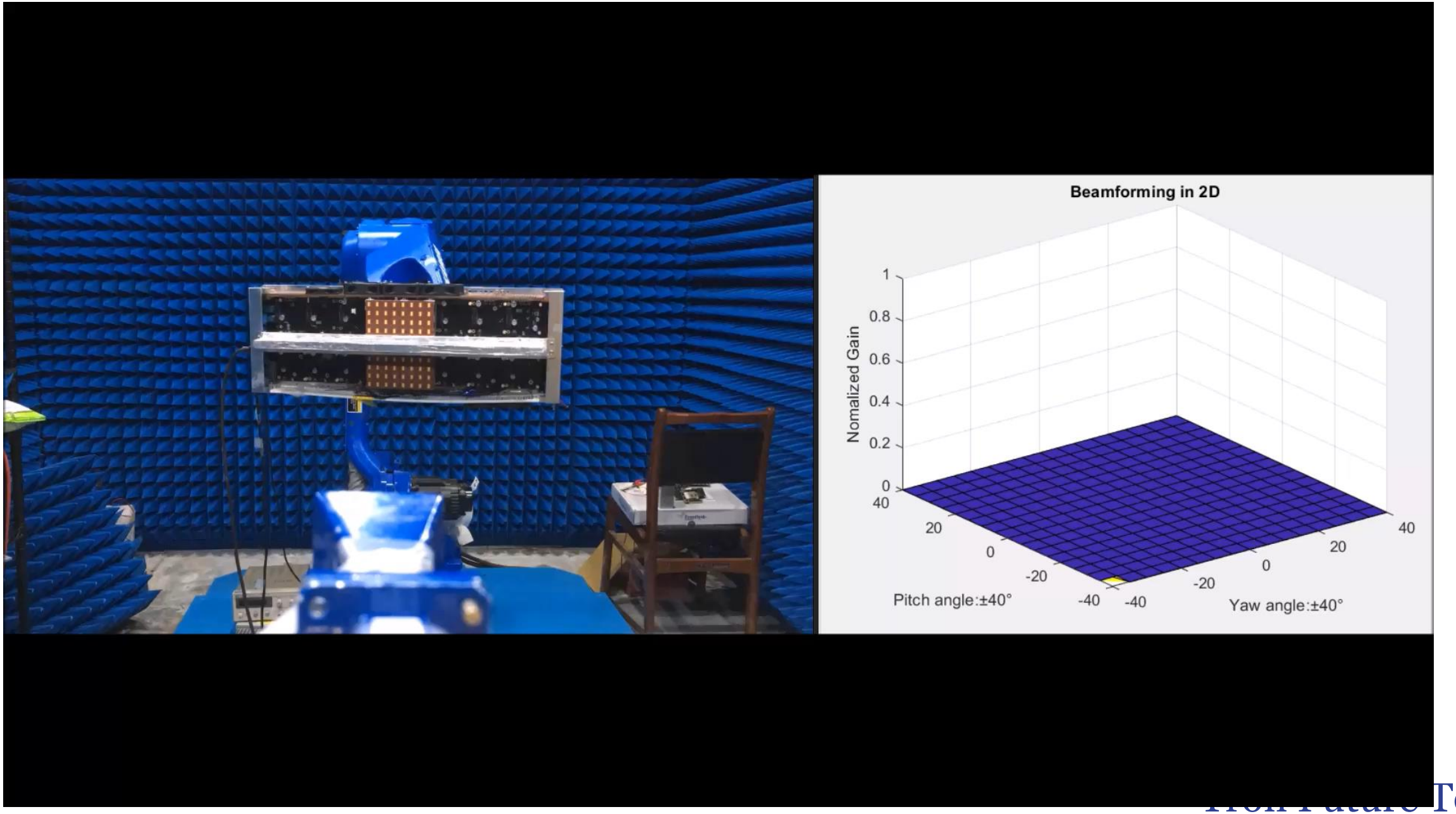
A Typical GaAs Frontend
PA Power: 27 dBm
LNA Gain: 16 dB
LNA NF: 2.5 dB
Switch Time : 1ns

CMOS RF SoC	
Transmitter	Receiver
Digital Input RF Output	RF Input Digital Output
Synchronized CLK Distribution	

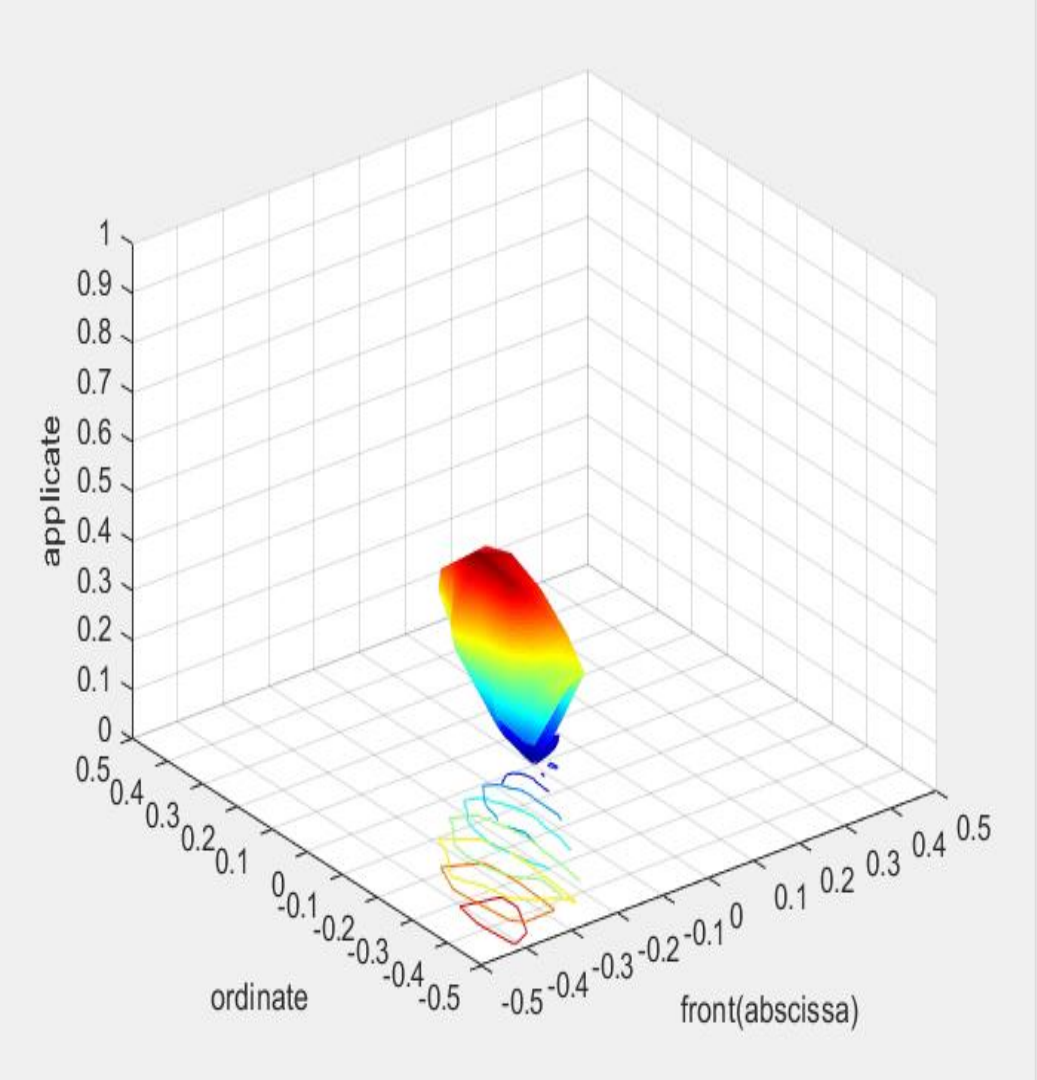
Package Size
15.3mm x 15.3 mm x 3mm 2.6mm (assembled thickness)

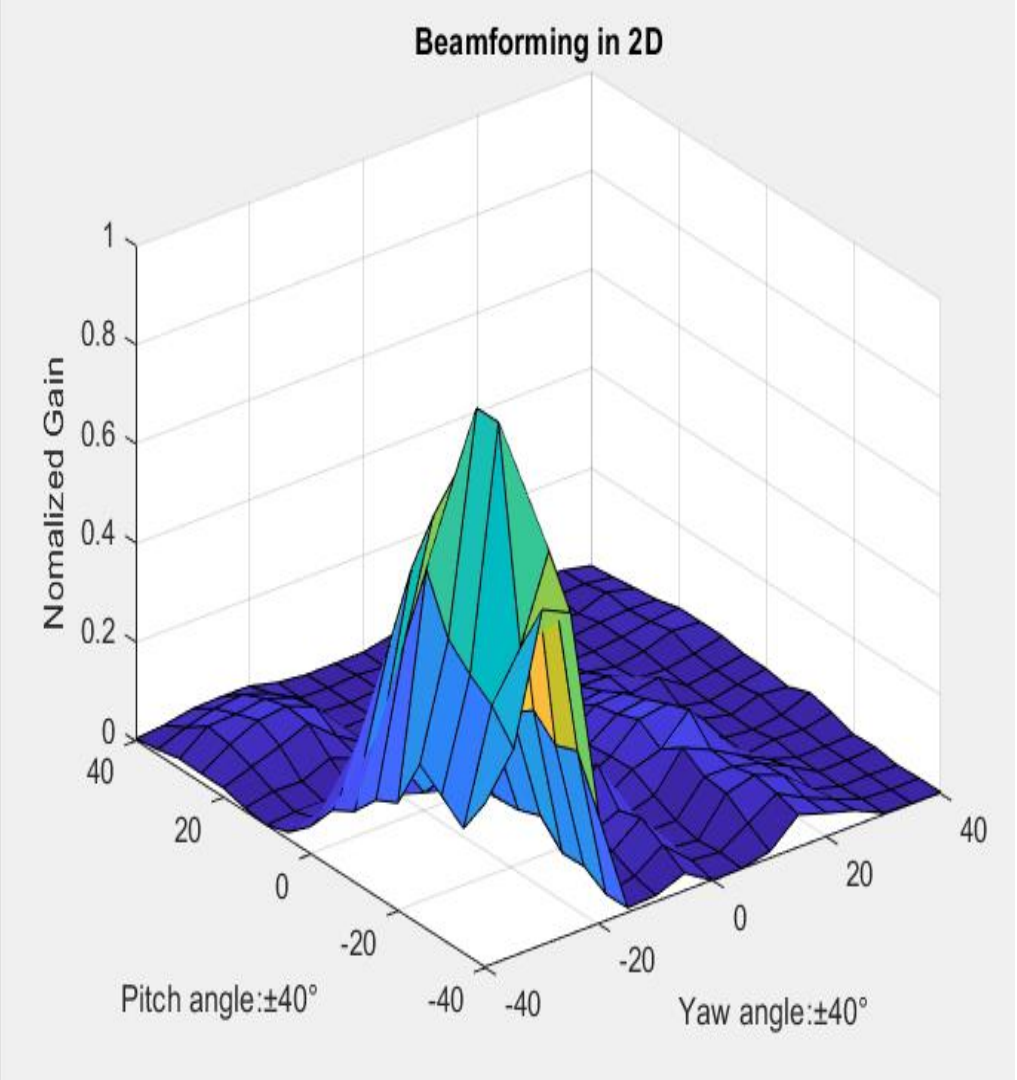
- The RF SoC can work with several GaAs and GaN frontends (LNA/PA).
- Production test approaches are proposed and reported in PIERS 2018.

4x8 Array Pattern Measurement



4x8 Sequential Scanning Pattern





- **Measured peak EIRP ~ 48 dBm with 32 CMOS only TXs.**
- **Expected: 66dBm with 32 CMOS TXs + 32 GaN PAs.**

Technical Details published in IEEE Radar Conference 2019.

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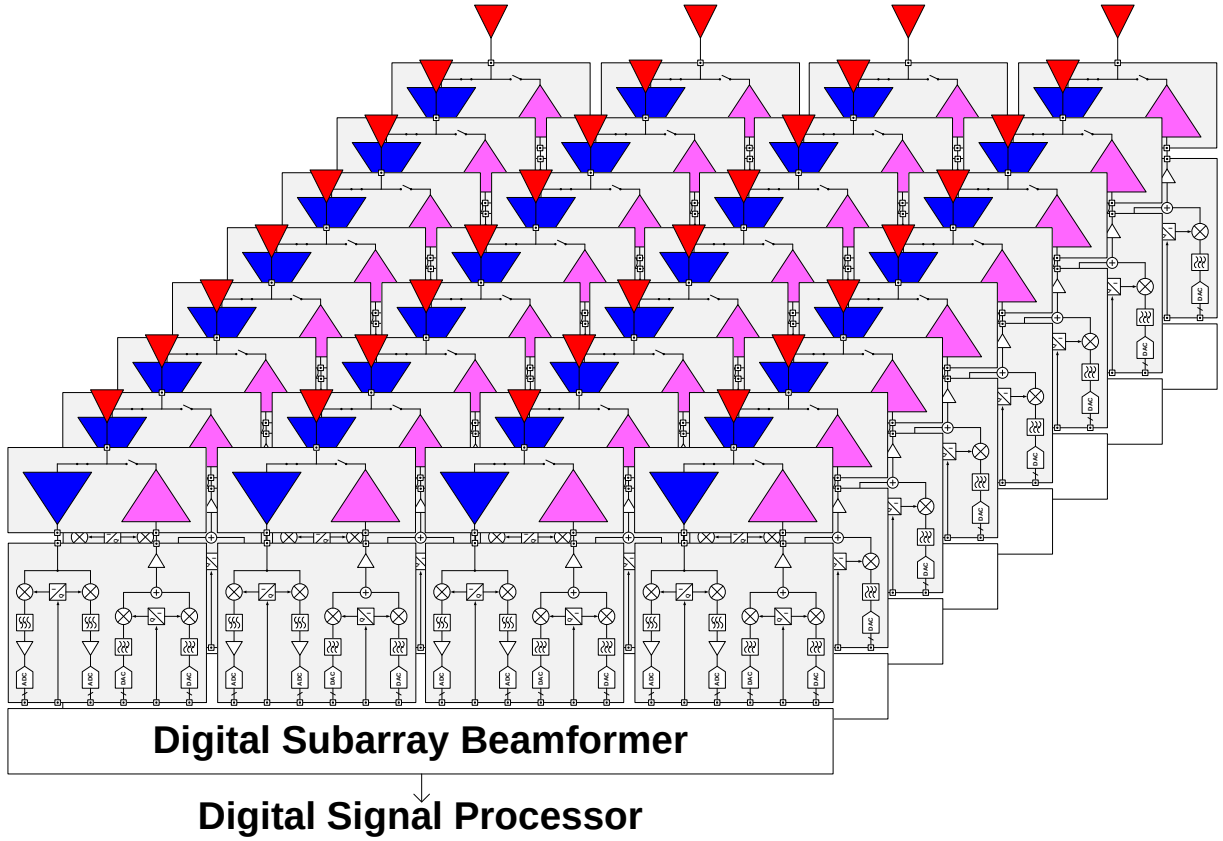
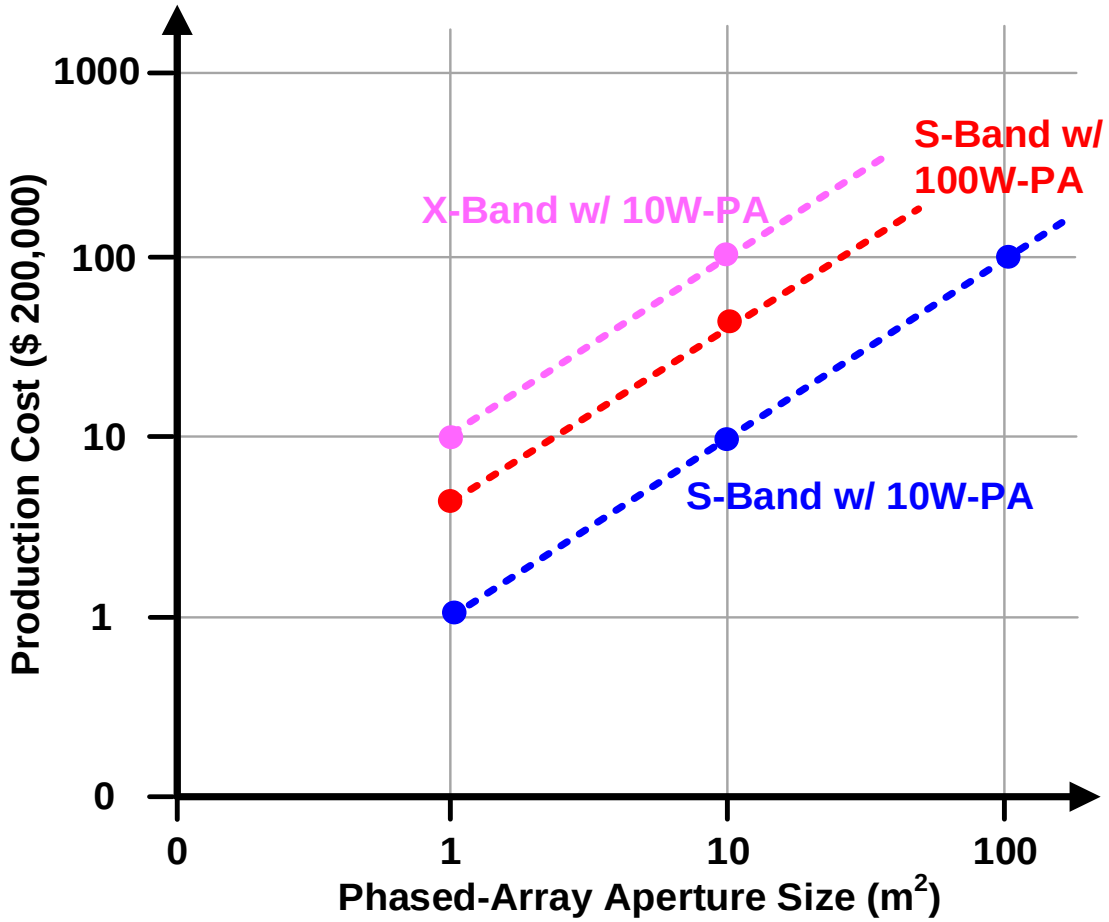
AESA Radar Cost Source: (1) Phased Array

Phased Array Structure



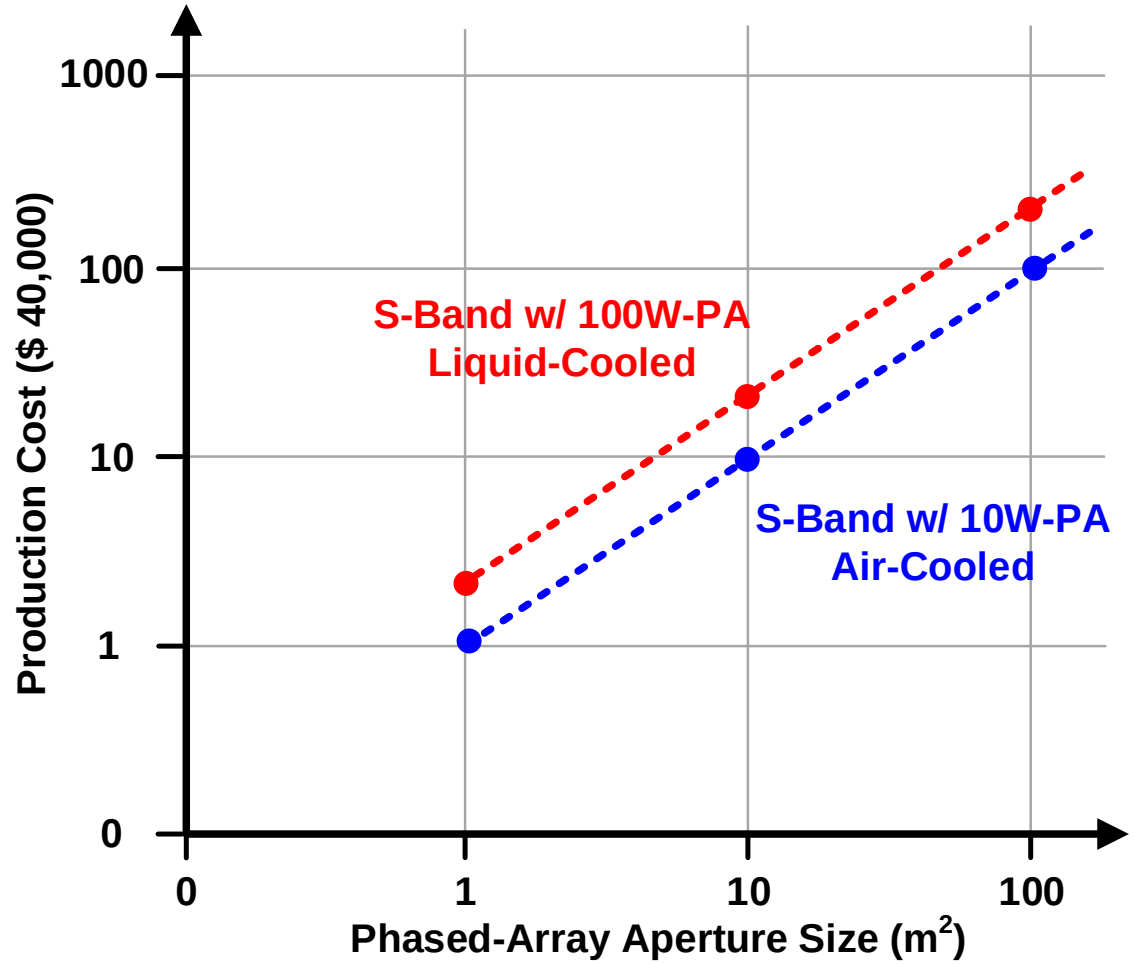
Phased array is a highly repetitive structure.
The performance is proportional to the array size.



The cost of phased array is proportional to the total no. of array elements and PA power.

[Ref] Herd J.S., Conway M.D. The Evolution to Modern Phased Array Architectures. *Proceedings of the IEEE*, 2016, Vol. 104, No. 3, pp. 519-529.

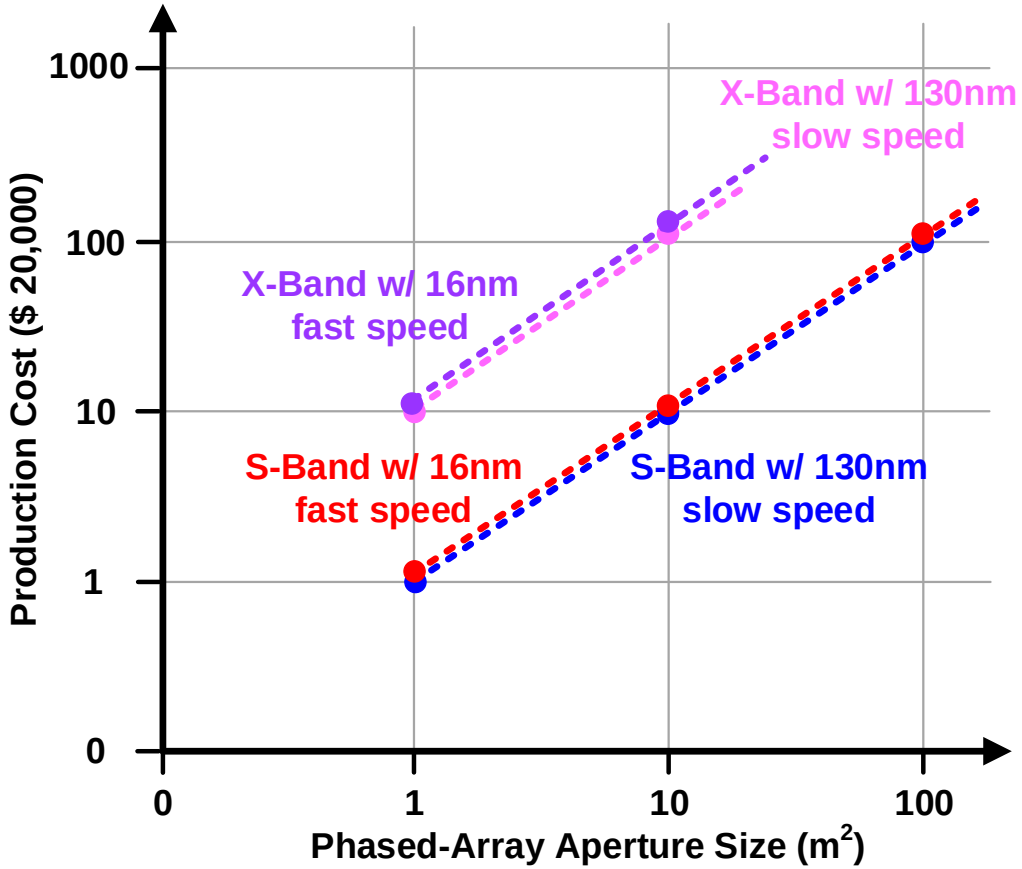
AESA Radar Cost Source: (2) Thermal Cooling



- Air-cooling has a heat density limit ~ 10kW/m^2.
- Liquid-cooling removes 20~50 times more heat with 4~10 times the cost.

[Ref] Herd J.S., Conway M.D. The Evolution to Modern Phased Array Architectures. *Proceedings of the IEEE*, 2016, Vol. 104, No. 3, pp. 519-529.

AESA Radar Cost Source: (3) Digital Processor

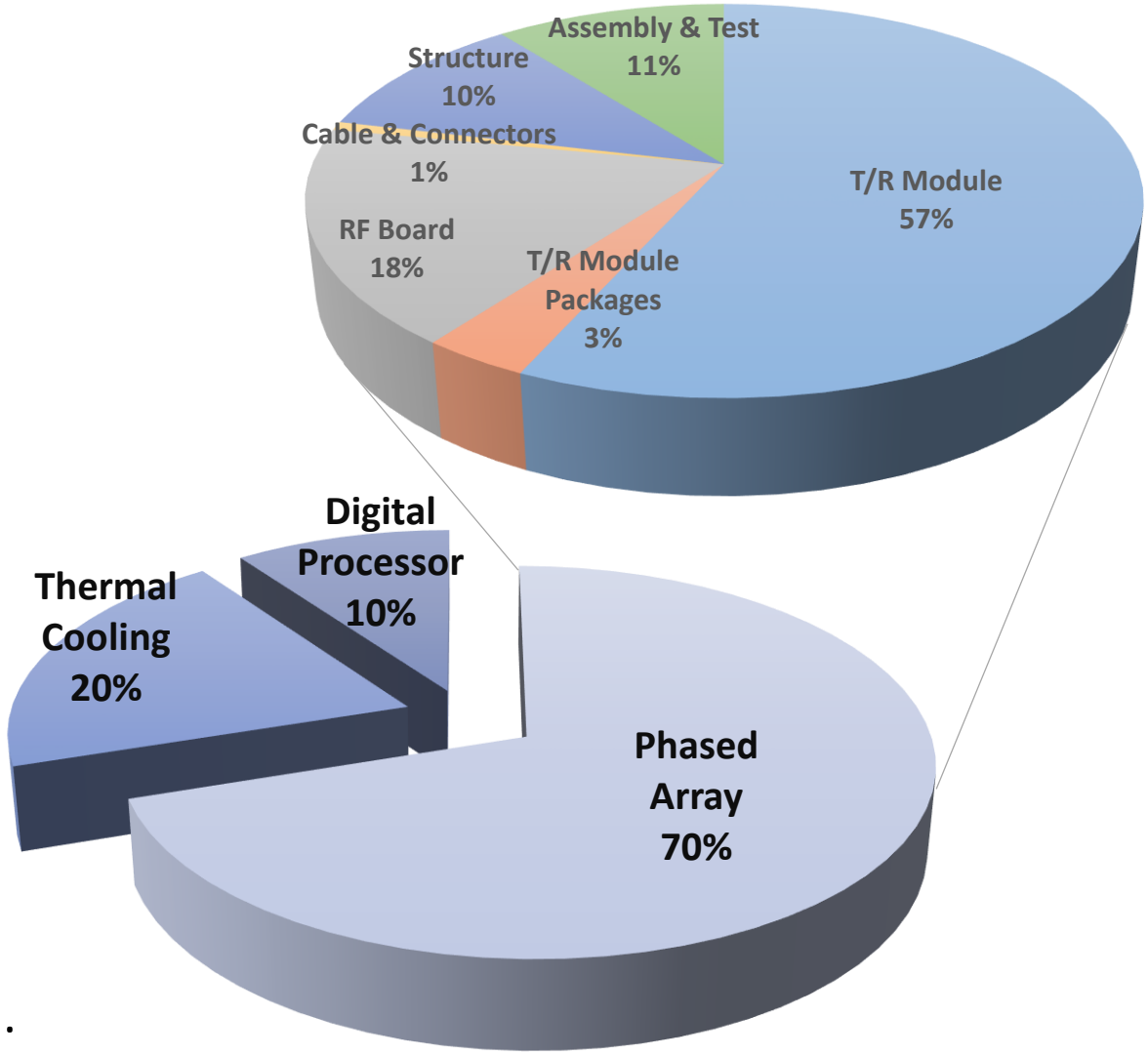


- Today's AESAs use Commercial Off-The-Shelf (COTS) devices such as FPGA, GPU, CPUs.
- Digital AESA will increase computing power requirements, but we get lots of additional benefits in return. We expect the processor cost to increase in the future.
- NRE cost for 130nm process is ~$200K, while 16nm > $3M.

AESA Radar Cost Structure Example

Tile Arrays at S-band with 10W-PA

Phased Array Radar Cost Sources		$/m^2	
Phased Array	T/R Module	$80,000	$14,000
	T/R Module Packages	$5,000	
	RF Board	$25,000	
	Cable & Connectors	$1,000	
	Structure	$15,000	
	Assembly & Test	$15,000	
Thermal Cooling			$40,000
Digital Processor			$20,000
Total			$200,000

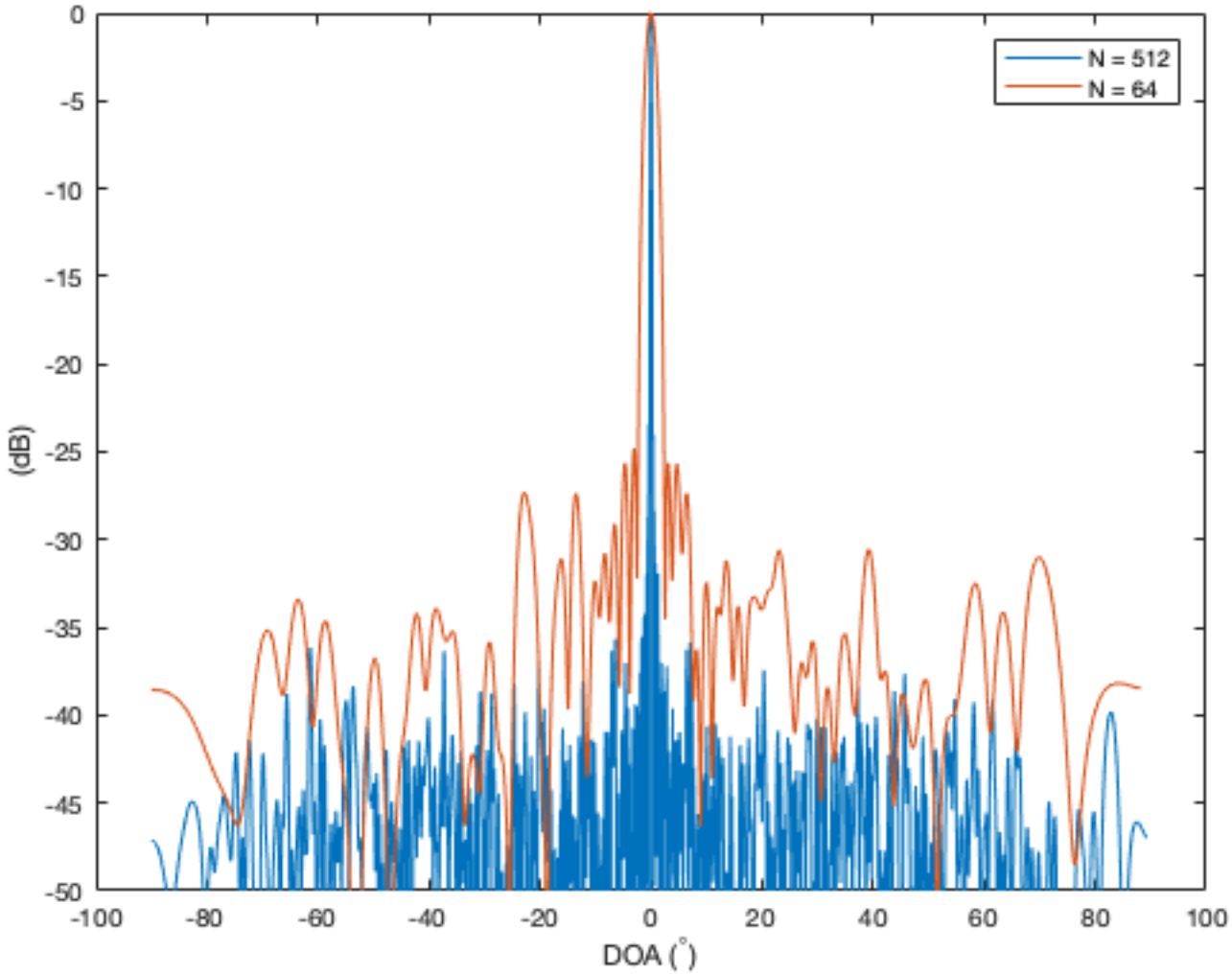


- Only hardware production cost is considered.
- Software, field test expenses and other NRE are not listed.
- To dramatically reduce AESA cost, we need to dramatically reduce no. of elements.

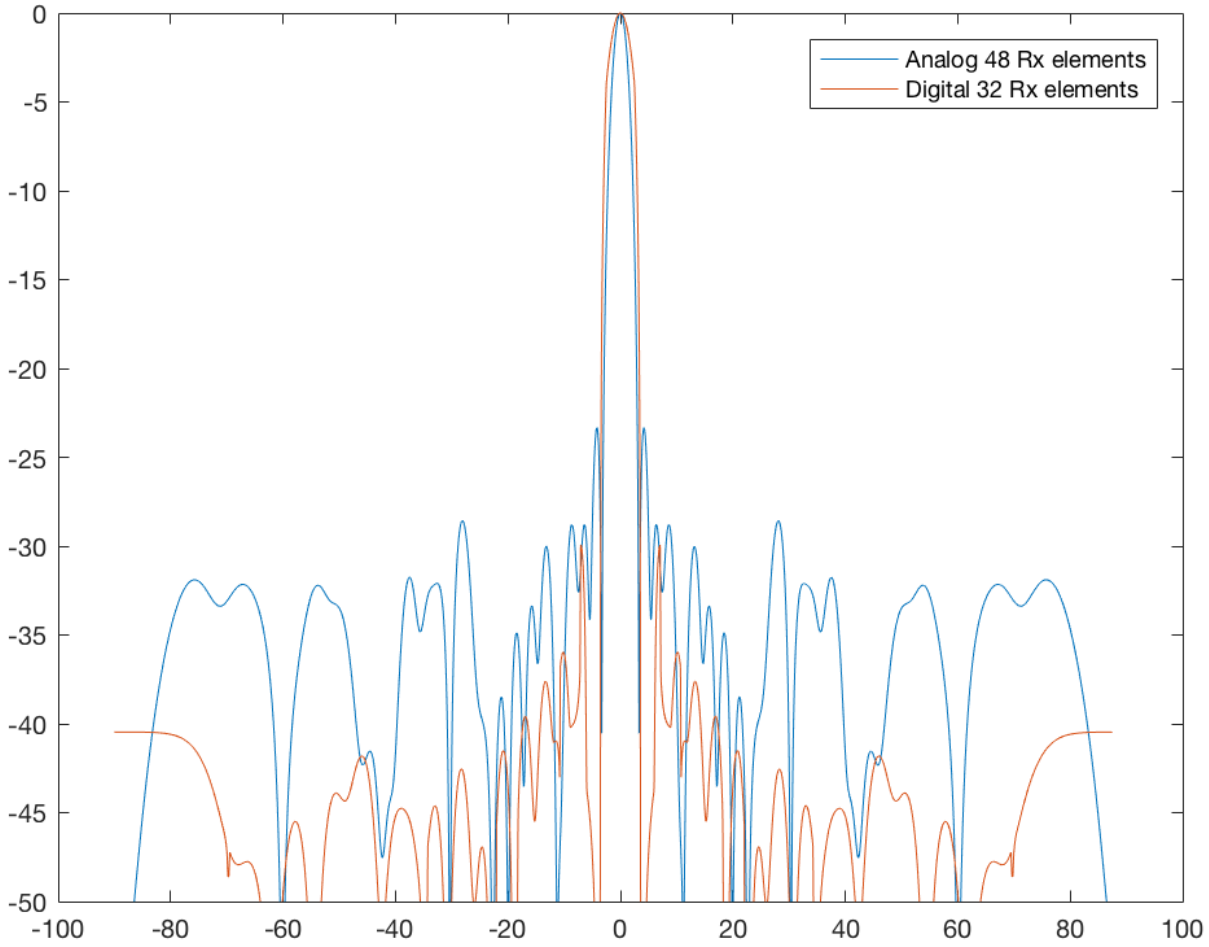
[Ref] Herd J.S., Conway M.D. The Evolution to Modern Phased Array Architectures. *Proceedings of the IEEE*, 2016, Vol. 104, No. 3, pp. 519-529.

Cost Reduction and Sidelobes Issues

- N=512 ➔ N=64
  - Peak Power Reduced.
  - Mainlobe beamwidth Increased .
  - Sidelobe Increased .
- Why sidelobes matter?
  - False targets.
- Though we can still distinguish range and velocity (MTI) bins.



Digital Beamforming v.s. Analog Beamforming



- Typical analog elementary errors:
  - $\pm$1dB amplitude variation, $\pm$3° phase error.
- All digital array achieve similar level of sidelobe rejection using 2~10 times less elements than analog counterparts.

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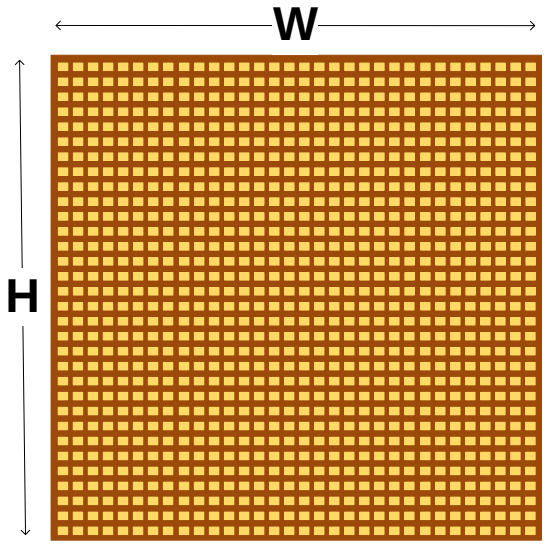
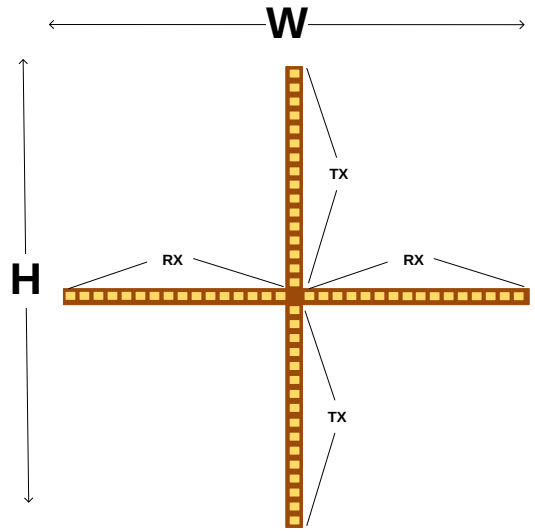
3D AESA Cost Reduction

- Fully Populated Planar AESA.
- Orthogonal Linear Digital AESA.



Comparable side-lobe suppression, mainlobe.



No. of Elements	W*H	H (TX), W (RX)	1024 ➔ 32 (3% cost)
Peak Power	$P_0 * W * H$	$\sim P_0 * (H)$	3% original power
Antenna Gain	$\propto W * H$	$\propto W$ (RX), $\propto H$ (TX)	3% gain for RX & TX
Max. Dwell Time	T_0	T_0* H	32 times with RX multibeam
SNR	SNR_0	$SNR_0 \cdot H/H^3$	1/1024 ➔ (18% detection range)
Cost per Area	C_0	C_0	Similar cost per coverage area.

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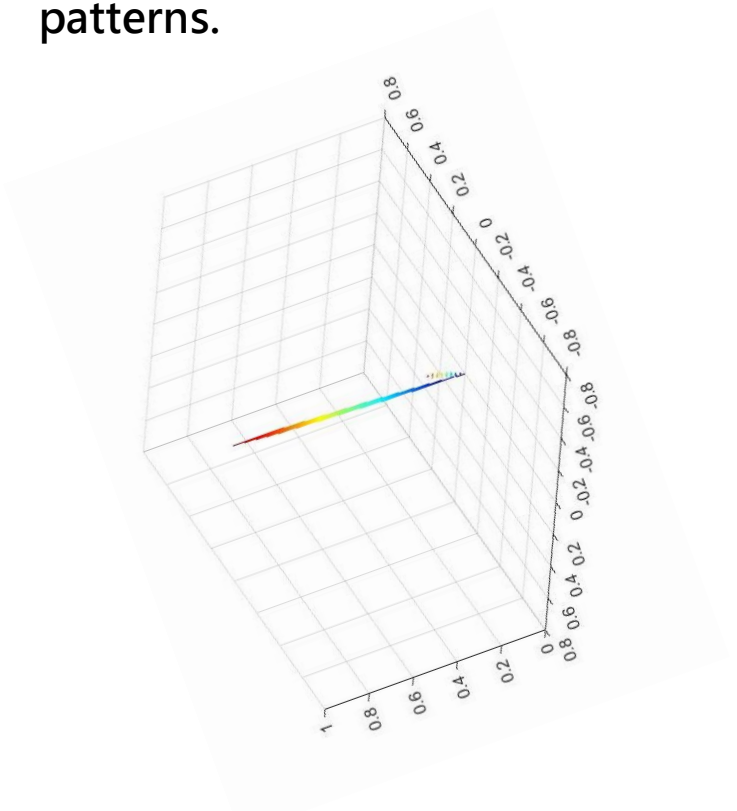
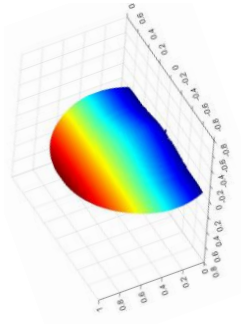
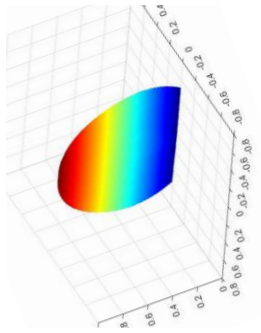
Basic Operational Concepts

- **Transmitter fan-shaped pattern.**
- **Receiver multi-beam pattern.**
- **Equivalent transmit-to-receive patterns.**







- Equivalent Radar Beam Pattern
- TX Vertical Scanning.
- RX Horizontal Multibeam Scanning.
- This is not the only operations, but a working example to show how it can work.

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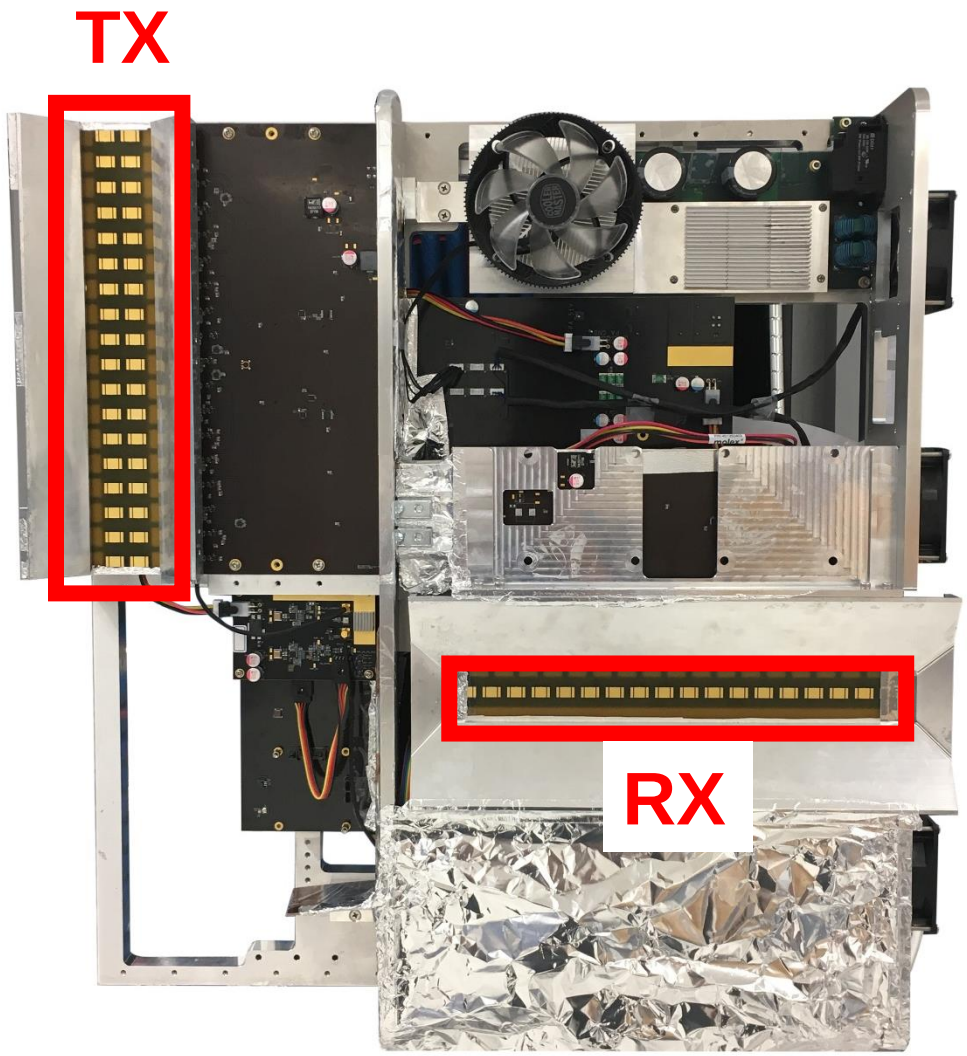
The Cost-Effective AESA Prototype



Specifications	
Number of Elements	1×16 TX (CMOS array with GaN PAs*) 1×16 RX (CMOS array with GaN LNAs*)
Architecture	Two hierarchy AESA
Frequency	8-9.5 GHz
Phase-shifting	All-digital
Applications	Radar/Communication/EW
Size (W/ Structure)	63 cm x 63 cm x 13 cm
Antenna Size (W/O Separator)	1×16 TX**: 31.7 cm x 7.03 cm 1×16 RX**: 31.7 cm x 7.75 cm
Weight (W/O Structure)	2.545 kg
Angular Scanning Range	$\pm 60°$ (RX) / $\pm 45°$(TX)
Peak EIRP	63 dBm
Only two external interface	1. AC Power: 90-230 VAC (Optional 20-60V VDC) 700W peak. 2. Ethernet.

* GaN PA: Qorvo TGA 2598; GaN LNA: Qorvo TGA 2512

** 1×16 frontend has two dummy antenna beside the main 16 antennas

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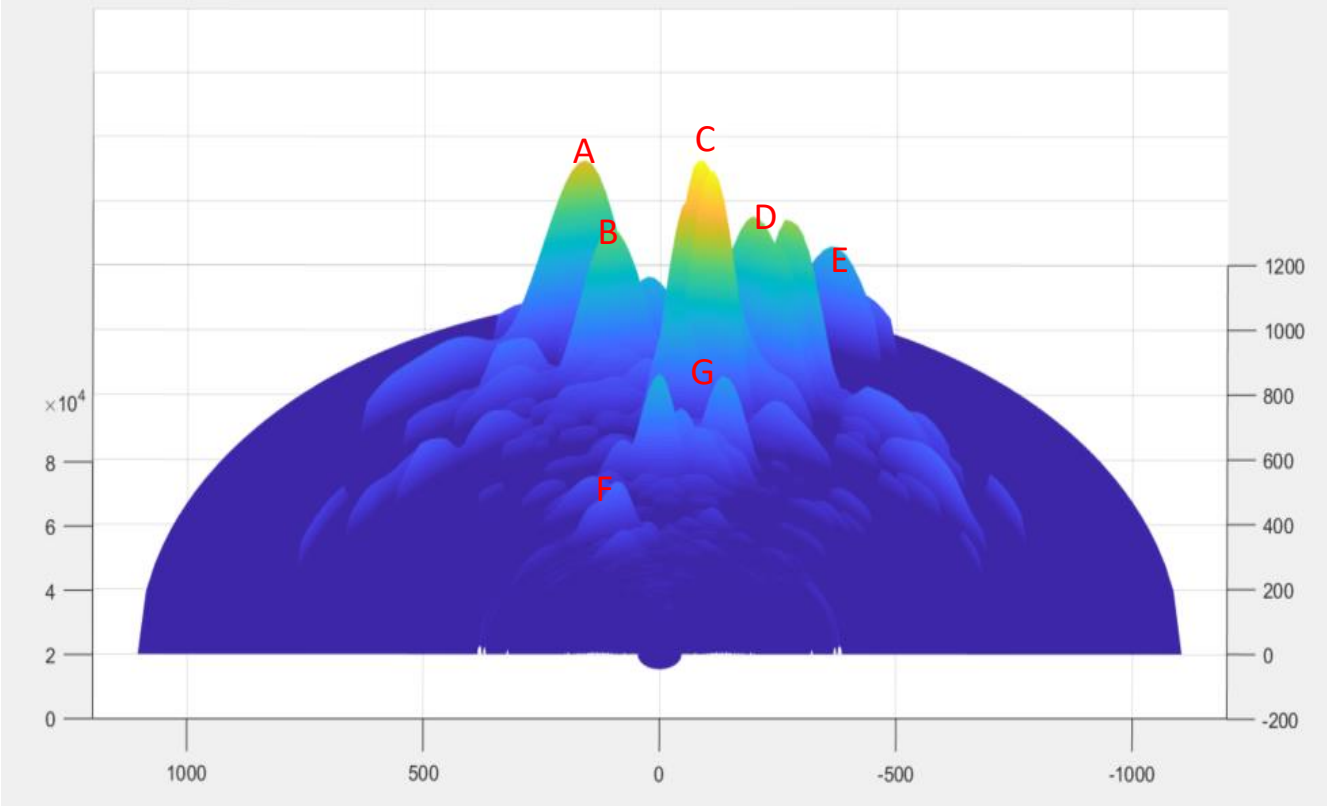
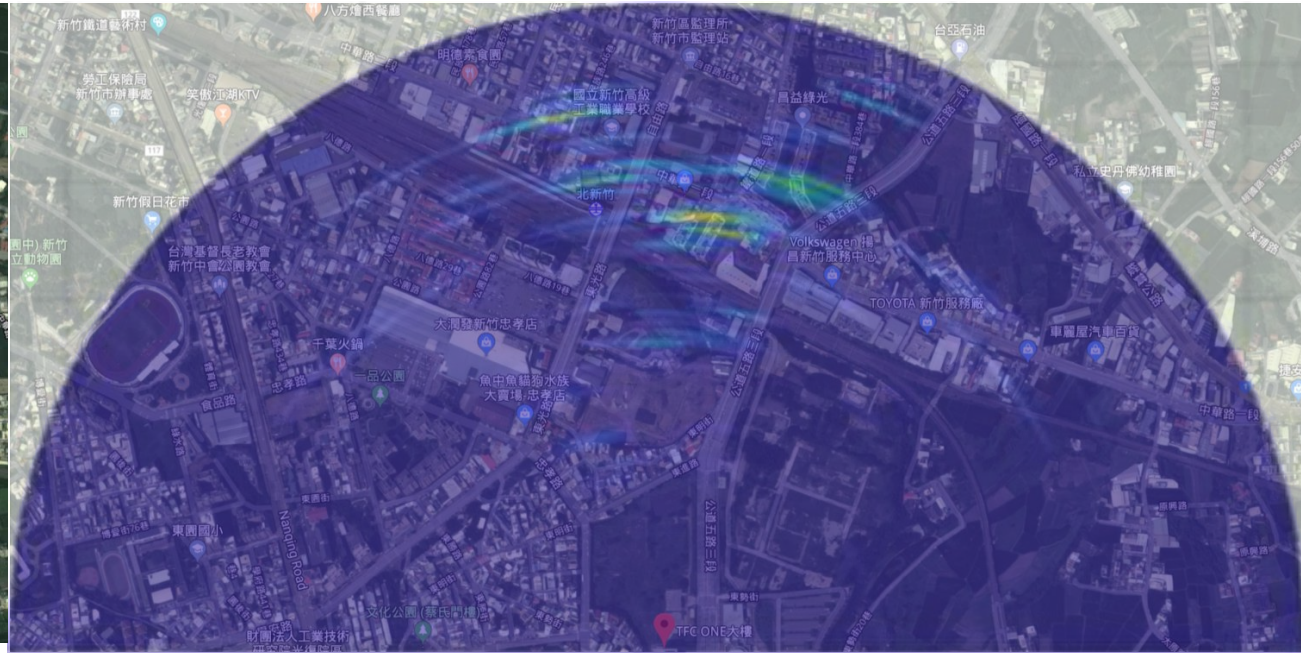
1TX 16RX LFM Multibeam Radar Experiments

- Distance: A=924m , B=808.5m, C=721.5m, D=831m, E=1101m, F=382.5m , G=530m



- This experiment used 1 TX and the 16-element RX array is located at 7F (around 35m from the ground).
- An absorber is used in front of the RX to limit the elevation angles so that close-in reflections from the ground are not received.
- The transmit pulse is 32 uSec LFM, and received signal is averaged by 64 PRIs, and then passes through the matched filter of the LFM signal.

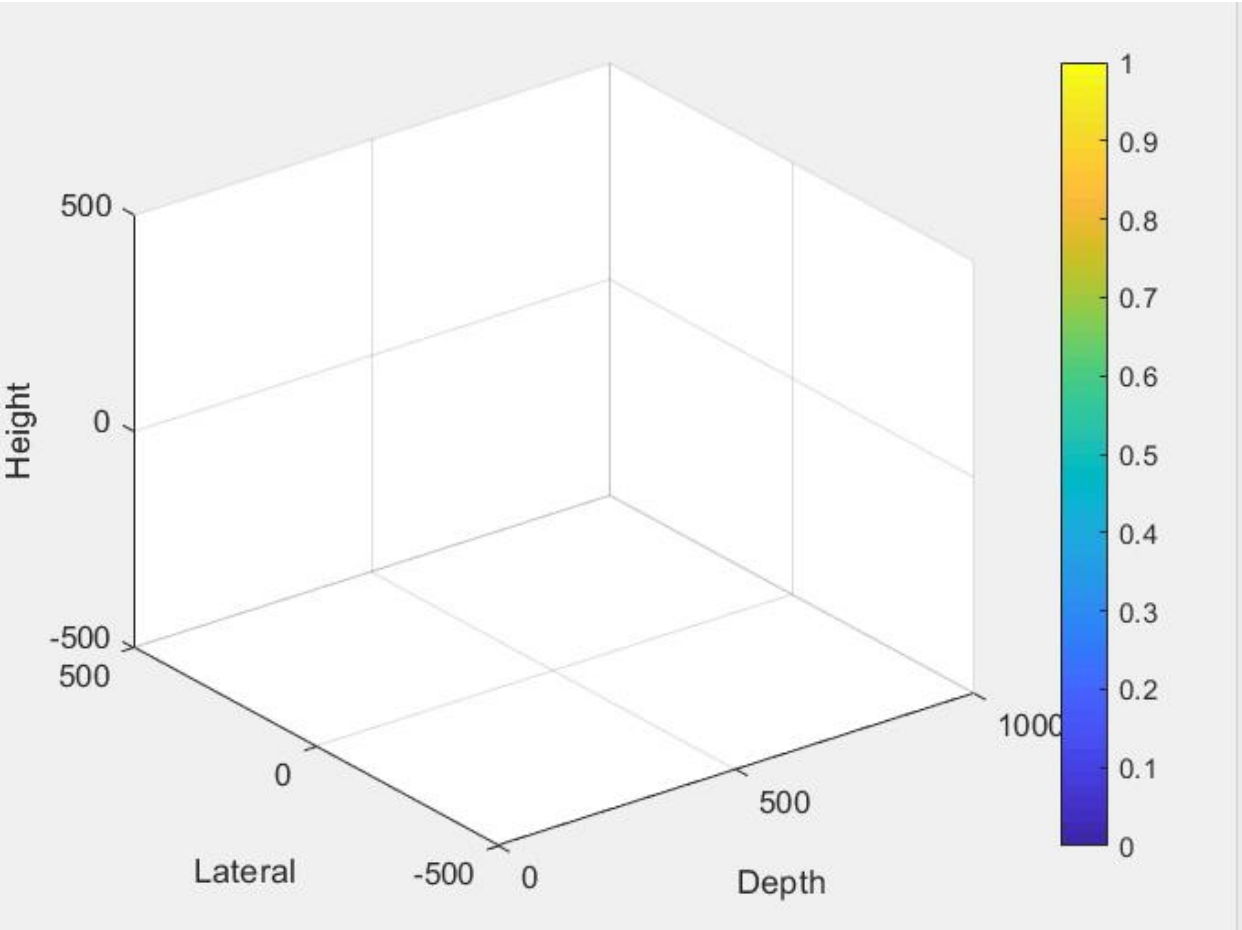
1TX 16RX LFM Multibeam Radar Experiments

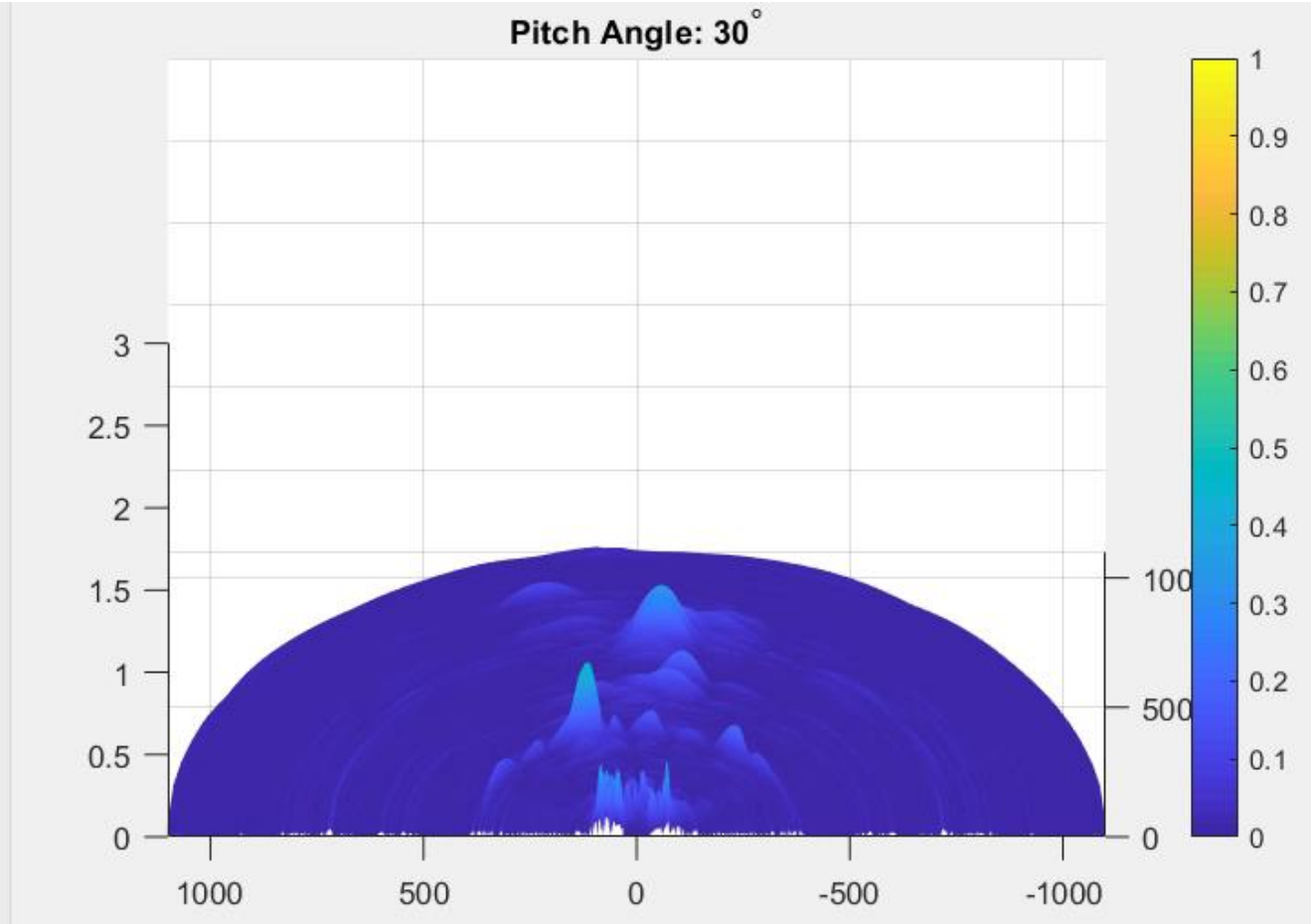


- From the top view, it is found that the light spots in the result plots of the experiment are perfected matched to the buildings shown on a map of the local are (map data from Google map).

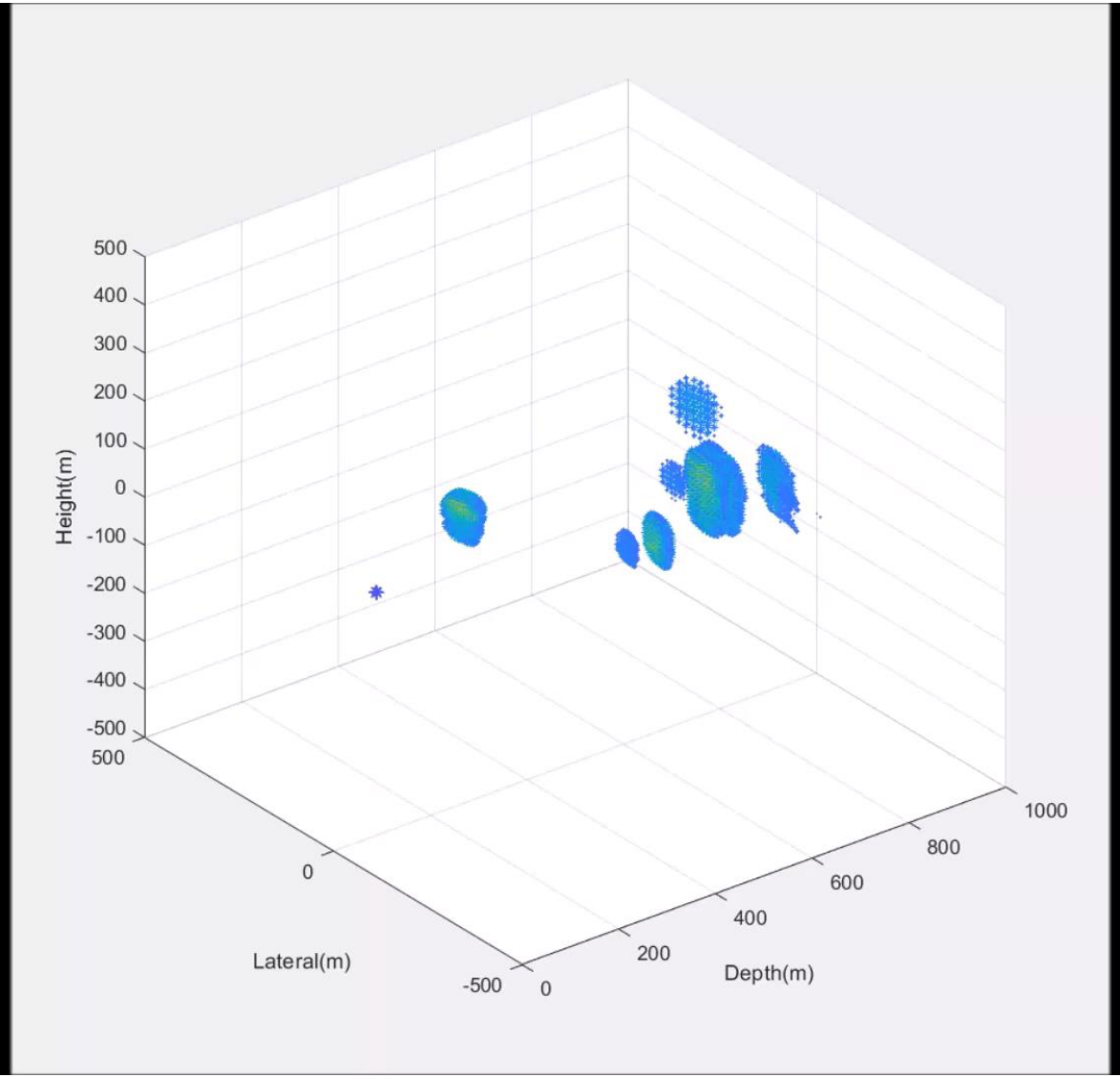
- The farthest range of this experiment is (768pt-32pt)*1.5 = 1104m.

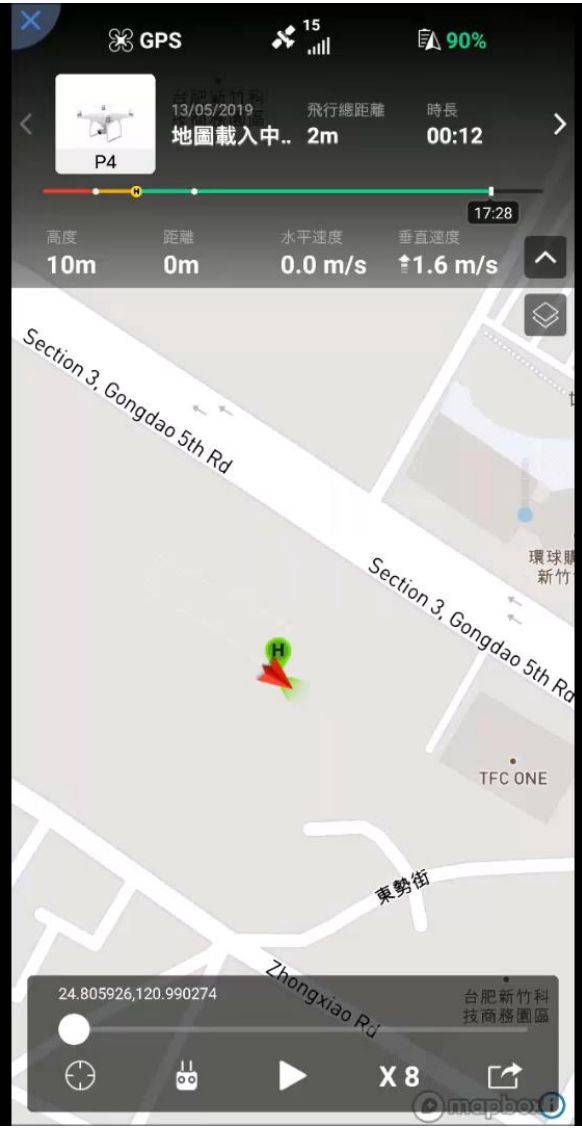
16TX 16RX 3D Surveillance Experiments





3D Drone Tracking Example





- Drone: DJI Phantom 4 (~0.01m^2 RCS)。

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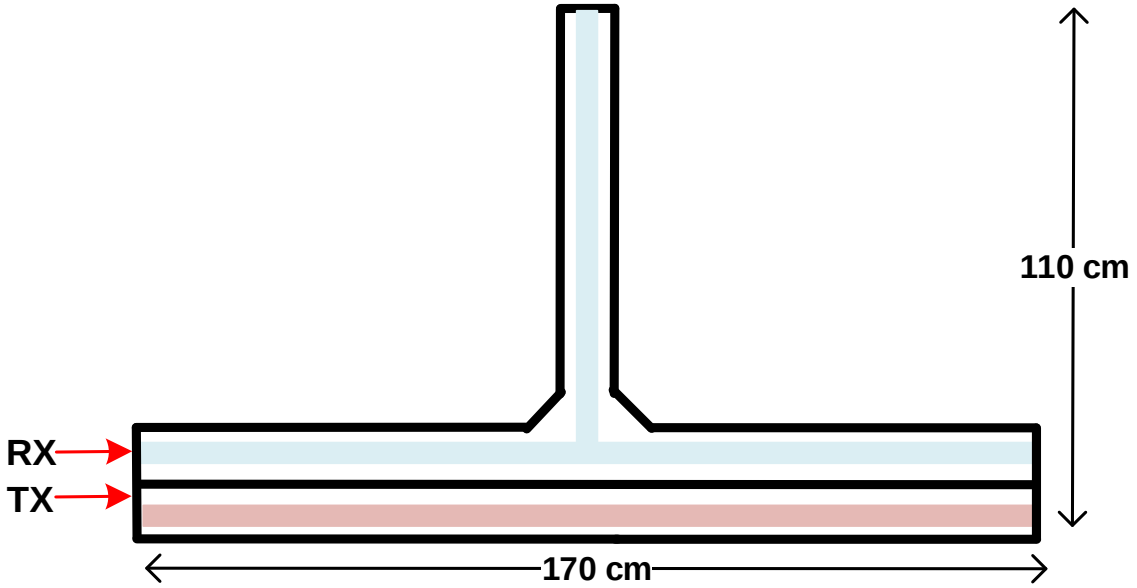
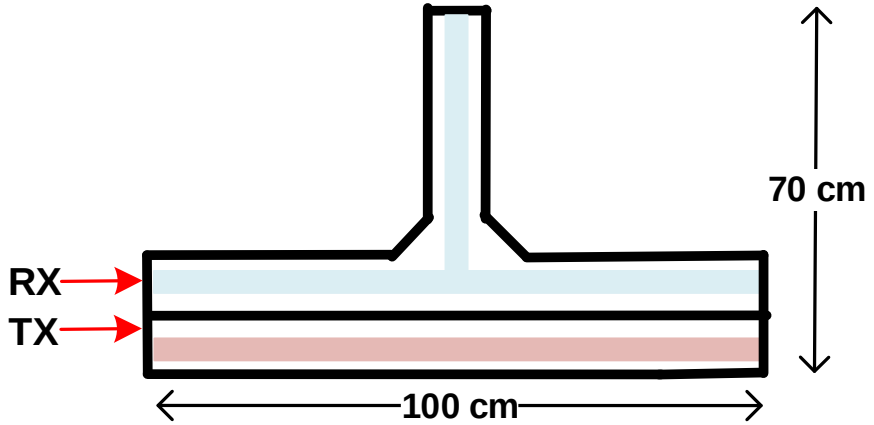
Most Likely S/X-band AESA Production Spec.

S-band (2.9-3.1GHz)



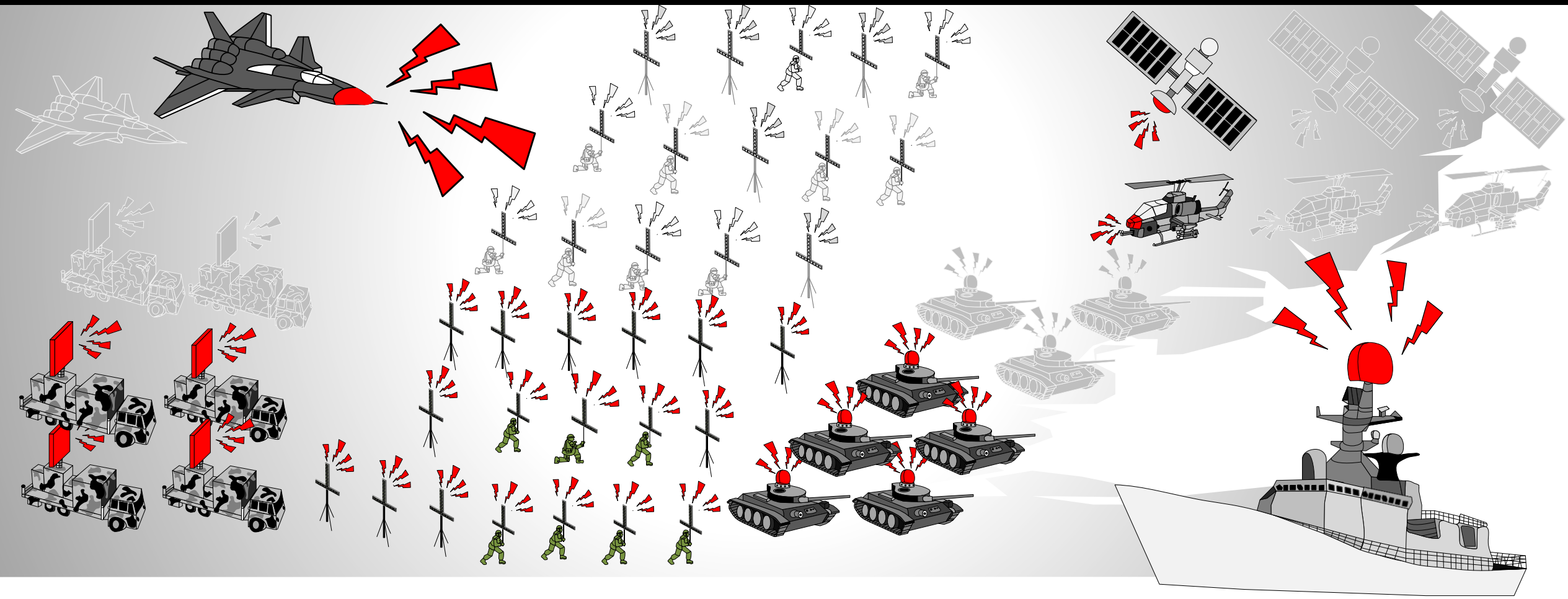
No. of Elements	32 TX, 32-48 RX (TBD)
Peak EIRP	25kW
Weight	<20kG
Est. Power Consumption	~200W
Beamwidth	3.5°(H), 7°(V)
Simulated Range	>20km@2m^2 , 2Hz Tracking
First Shipping for Field Test	Sept. 30, 2019

X-band (8.0-9.5GHz)



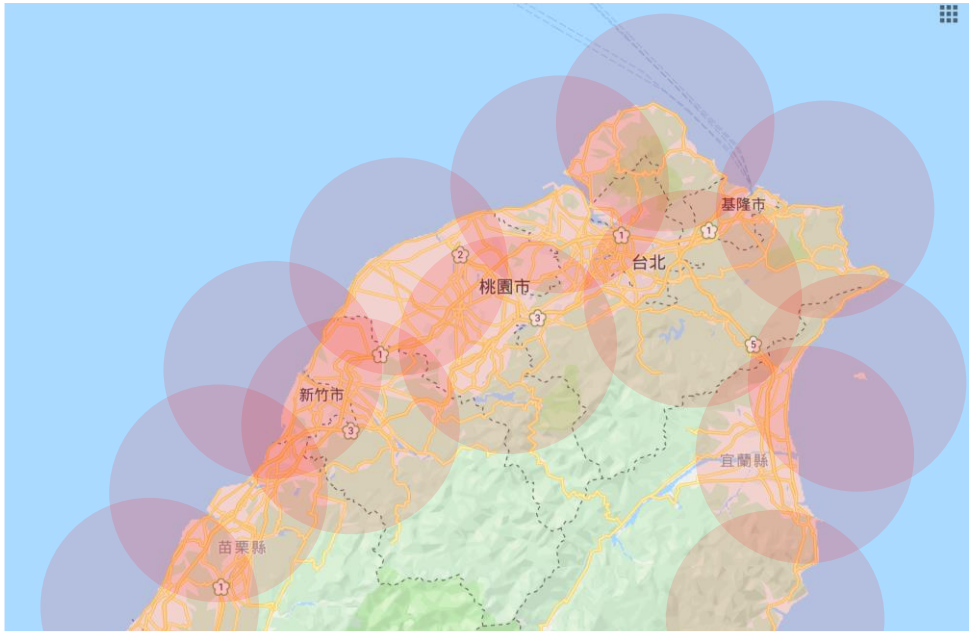
No. of Elements	64 TX, 64-96 RX (TBD)
Pea EIRP	20kW
Weight	<15kG
Est. Power Consumption	~150W (TBD)
Beamwidth	2°(H), 3.5°(V)
Simulated Range	>10km@2m^2 , 2Hz Tracking
First Shipping for Field Test	TBD

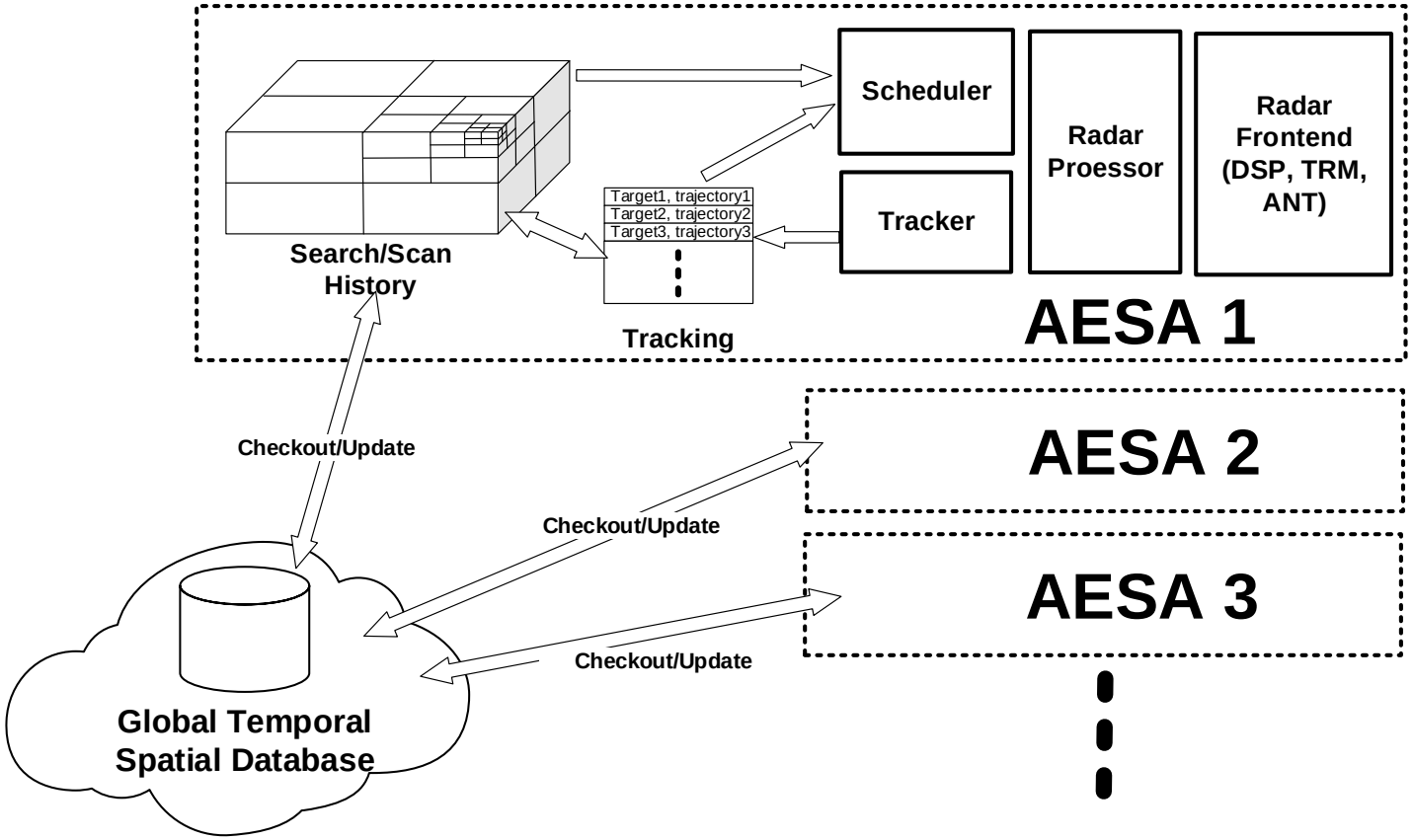
AESA in Future EW



- **Cost-effective AESAs begin to be pervasive to complement existing high-performance AESAs.**
- **Chip-scale atomic clocks enable massive software-defined AESA platform.**
- **Software is key to fully utilize the massive number of AESA.**

Software Architecture





- Global temporal-spatial database in the cloud keeps track of area being serviced and tracking data from each AESA.
- Each AESA checks out a region from the cloud, and run autonomously. Keep updating operating status to the cloud. The cloud arbiter/resolves any conflicts from each AESA.
- Cooperation between a large number of mobile AESA and conventional units while making the whole system resilient and robust with redundant units will be an important problem that needs to be extensively studied.

Conclusion

- AESA hardware cost is roughly proportional to array elements.
- Reducing array elements will reduce peak power (range), increase mainlobe beamwidth (number of identified targets), and reduce sidelobe rejection. Side-lobe rejection is important for preventing false targets.
- Digital AESA has a much better sidelobe rejection than an analog counterpart.
- Use of orthogonal linear AESAs can create a virtual 2D AESA, but a much smaller number of array elements.
- Reducing array elements, and highly integrated T/R module, we can make mid/short-range AESA light-weight and cost-effective **today**.
- EW community enters a new era of massive number of AESAs.

Q & A

- Critiques, questions, and suggestions are highly welcome.
- Thank you for your attentions.
- Email: yw@tronfuturetech.com

TRON FUTURE TECH

Yu-Jiu Wang

Chairman & Chief Executive Officer
Ph.D., California Institute of Technology
Director of Taiwan Space Industry Development Association
National Industrial Innovation Award, ROC

7F-A, No.1, Sec.3, Gongdao 5th Rd.
Hsinchu 300, Taiwan (R.O.C)
+886-3-575-0057, +886-928-126-750
yw@tronfuturetech.com www.tronfuturetech.com